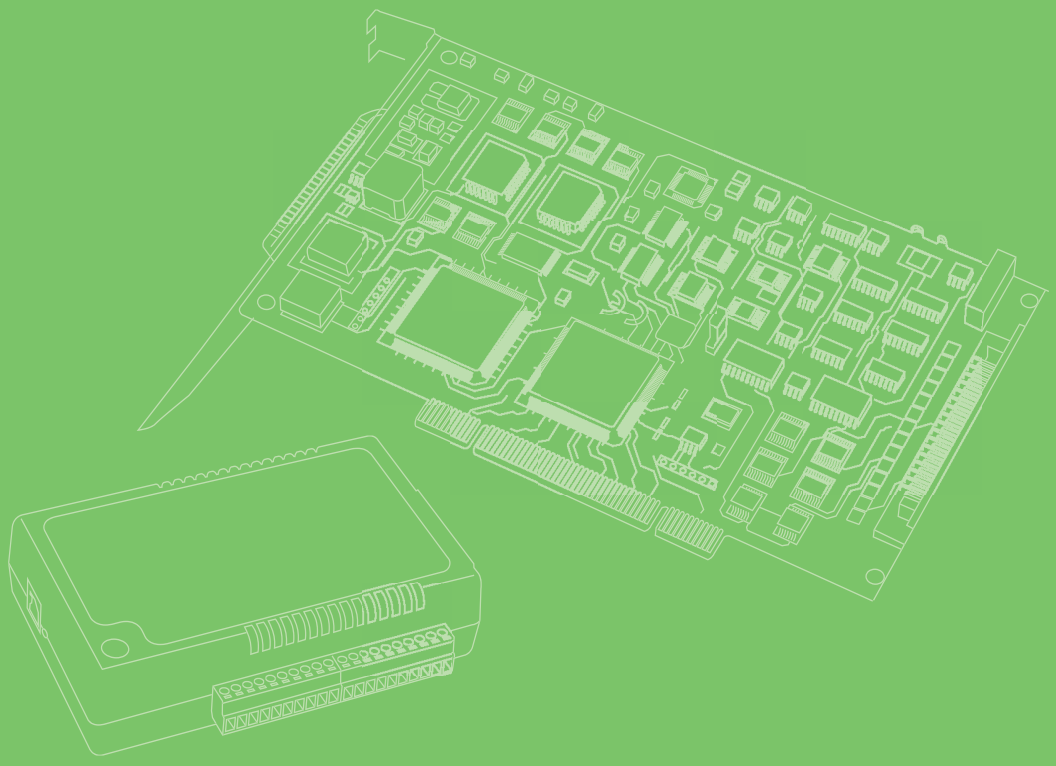


User Manual

PCIE-1813

38.4 kS/s, 26-Bit, 4-Ch, Simultaneous Sampling, Universal Bridge Input, Multifunction PCI Express Card

ADVANTECH

Enabling an Intelligent Planet

Copyright

Acknowledgments

Intel and Pentium are trademarks of Intel Corporation.

Microsoft Windows and MS-DOS are registered trademarks of Microsoft Corp.

All other product names or trademarks are properties of their respective owners.

Product Warranty (2 years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, users are billed according to the cost of replacement materials, service time, and freight. Consult your dealer for more details.

If you suspect that your product is defective, follow the steps outlined below:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any on-screen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the packaging and ship the package prepaid to your dealer.

Part No. 2001181311 Edition 2

Printed in Taiwan May 2020

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. Such cables are available from Advantech. Please contact your local supplier for ordering information.

Technical Support and Assistance

1. Visit the Advantech website at **http://support.advantech.com.tw/** to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A comprehensive description of the problem
   - The exact wording of any error messages

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any of the items are missing or damaged, contact your dealer immediately.

- 1 x PCIE-1813 DA&C card
- 1 x user manual
- 1 x DVD-ROM with DAQ Navi drivers

Safety Precautions - Static Electricity

Follow the simple precautions below to protect yourself from harm and the products from damage.

1. To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards when the PC is powered on.
2. Disconnect the power before implementing any configuration changes. The sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.

Contents

Chapter 1

Introduction

This chapter introduces PCIE-1813 and its typical applications.

- Features
- Applications
- Installation Guide
- Software Overview
- Roadmap
- Accessories

The PCIE-1813 is a 26-bit high-resolution multi-function data acquisition PCI Express card which integrates 4-ch analog inputs, 2-ch analog outputs, 32-ch digital I/Os, and 4 encoder (or general purpose) counters.

- 26-bit AI conversion (voltage and universal bridge input)
- 16-bit AO conversion
- Digital input
- Digital output
- Encoder counter/ Timer

PCIE-1813 is an advanced high-performance multifunction card based on the PCIe x1 Bus. With a large FIFO of 1K Sample, the maximum sampling rate of PCIE-1813 is up to 38.4 KS/s with 4 A/D converters simultaneously sampling on each channel. The PCIE-1813 has two 16-bit D/A output channels, 32 digital input/output channels, and four 32-bit Time/counter channels so that it can provide specific functions for different application requirements.

1.1 Features

- Four differential simultaneous sampling voltage and universal inputs
- 26-bit AI converter, up to 38.4 kS/s sampling rate for each channel
- Start-, Delay to Start-, Delay to Stop-, Stop-event trigger capable
- Programmable gain for each input channel
- 1K and 8K onboard buffer for analog input and analog output respectively
- Two independent 16-bit analog output channels with continuous waveform output function of maximum 3 MHz throughput rate
- Auto-calibration for analog input and output channels
- System calibration for bridge input signals
- 32 digital Input or output channels, TTL compatible
- Four 32-bit independent encoder (or general purpose) counters
- BoardID switch

PCIE-1813 offers the following main features:

PCIe-Bus Plug & Play

The PCIE-1813 card uses a PCIe controller to interface the card to the PCI Express bus. The controller fully implements the PCI Express Base Specification v1.1. All configurations related to the bus, such as base address and interrupt assignment, are automatically controlled by software. No jumper or switch is required for user configuration.

Four A/D Converters for Simultaneous Sampling

PCIE-1813 card is capable of simultaneous sampling with dedicated A/D converter circuit for each analog input channel.

Onboard Buffer Memory

There are 1K and 8K sample buffers for AI and AO respectively on PCIE-1813. This is an important feature for faster data transfer and more predictable performance under Windows systems.

Onboard Programmable Encoder (or General Purpose) Counters

The PCIE-1813 features four 32-bit encoder (or general purpose) counters to provide encoder input, encoder compare output, one shot output, PWM output, periodic interrupt output, time-delay output, and the measurement of frequency and pulse width.

BoardID Switch

The PCIE-1813 has a built-in DIP switch that helps define each card's ID when multiple PCIE-1813 cards have been installed on the same PC chassis. The BoardID setting function is very useful when building a system with multiple PCIE-1813 cards. With the correct BoardID settings, you can easily identify and access each card during hardware configuration and software programming.

Note! *For detailed specifications and operations of PCIE-1813, please refer to Appendices A and B.*

1.2 Applications

- Load cell and strain gauge measurements
- Waveform acquisition and analysis
- Process control and monitoring

1.3 Installation Guide

Before you install your PCIE-1813 card, please make sure you have the following necessary components:

- PCIE-1813 DA&C card
- PCIE-1813 User Manual
- Driver software Advantech DAQNavi software (included in the companion DVD-ROM)
- Personal computer or workstation with a PCI Express interface (running Windows 10, 8 and 7)
- Shielded Cable PCL-101100R (optional)
- Wiring Board ADAM-39100 (optional)

Other optional components are also available for enhanced operation:

- DAQ Navi, LabView or other 3rd-party software

After you get the necessary components and maybe some of the accessories for enhanced operation of your multifunction card, you can then begin the installation procedure. Figure 1.1 on the next page provides the broad installation steps:

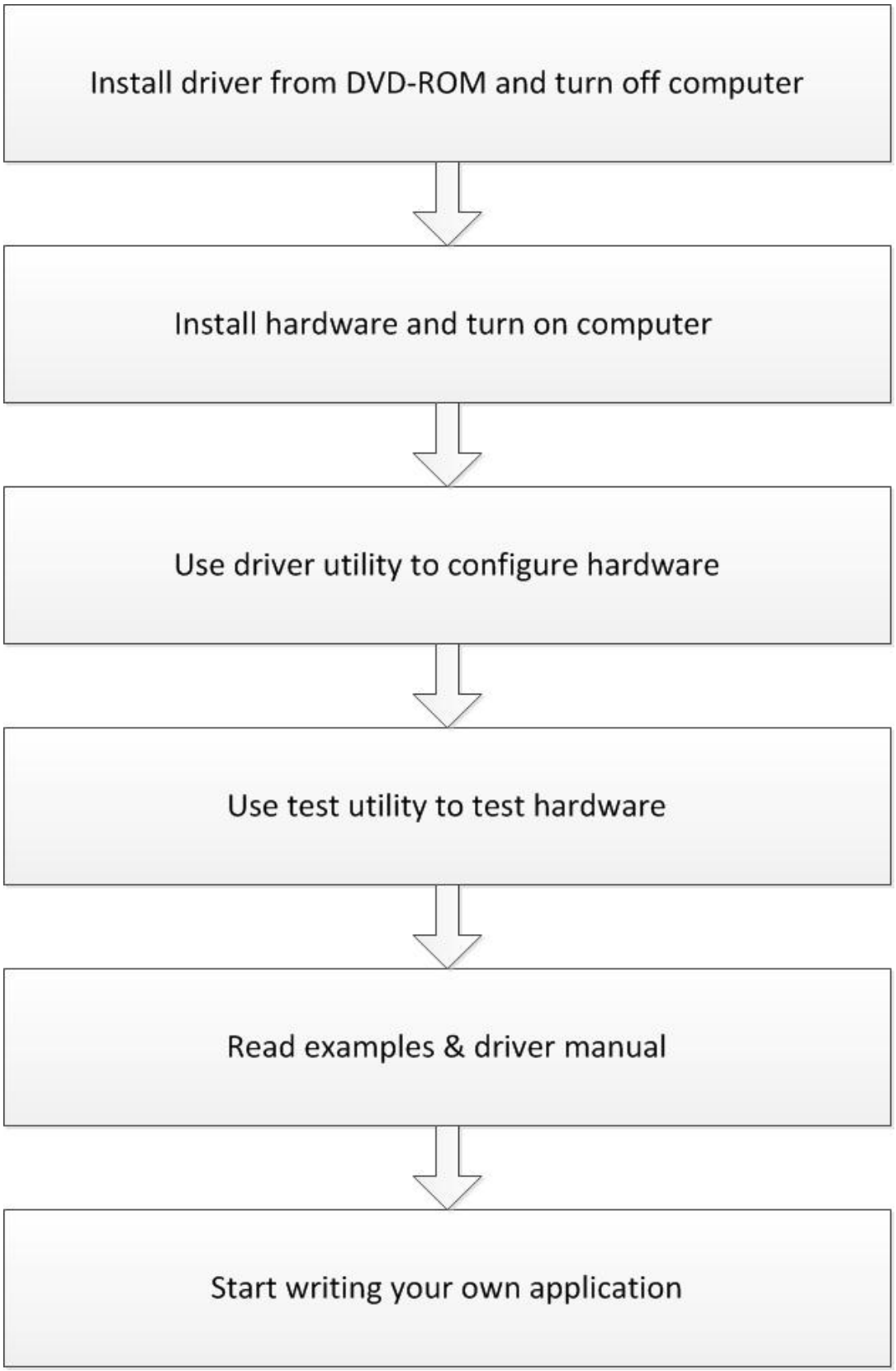


Figure 1.1 Installation flowchart

1.4 Software Overview

Advantech offers a rich set of DLL drivers, third-party driver support, and application software to help fully exploit the functions of your PCIE-1813 card:

- Device Drivers (on the companion DVD-ROM)
- LabVIEW driver
- Advantech DAQNavi
- Data logger

Programming Choices for DA&C Cards

You may use Advantech application software such as Advantech Device Drivers. On the other hand, advanced users can use register-level programming, although this is not recommended due to its laborious and time-consuming nature.

DAQNavi Software

Advantech DAQNavi software includes device drivers and an SDK, which features a complete I/O function library to help boost your application performance. This software is included in the companion DVD-ROM at no extra charge and comes with all Advantech DA&C cards. The Advantech DAQNavi software for Windows XP/7/8 (desktop mode) works seamlessly with development tools such as Visual Studio .NET, Visual C++, Visual Basic and Borland Delphi.

1.5 DAQNavi Device Driver Programming Roadmap

This section will provide you with a roadmap to demonstrate how to build an application from scratch using Advantech DAQNavi Device Driver with your favorite development tools such as Visual Studio .NET, Visual C++, Visual Basic, Delphi, and C++ Builder. The step-by-step instructions on how to build your own applications using each development tool is given in the Device Drivers Manual. A rich set of example source code is also provided for your reference.

Programming Tools

Programmers can develop application programs with their favorite development tools:

- Visual Studio .NET
- Visual C++ and Visual Basic
- Delphi
- C++ Builder

For instructions on how to begin programming work in each development tool, Advantech offers a Tutorial Chapter in the *DAQNavi SDK Manual* for your reference. Please refer to the corresponding sections in this chapter on the *DAQNavi SDK Manual* to begin your programming effort. You can also look at the example source code provided for each programming tool; examples can help jump-start a project.

The *DAQNavi SDK Manual* can be found on the companion DVD-ROM. Alternatively, if you have already installed the Device Drivers on your system, The *DAQNavi SDK Manual* can be readily accessed through the Start button:

Start/Programs/Advantech Automation/DAQNavi/DAQNavi Manuals/DAQNavi SDK Manual

The example source code can be found under the corresponding installation folder such as the default installation path:

\Advantech\DAQNavi\Examples

For information about using other function groups or other development tools, please refer to the Using DAQNavi SDK chapter in the DAQNavi SDK Manual, or the video tutorials in the Advantech Navigator.

Programming with DAQNavi Device Drivers Function Library

Advantech DAQNavi Device Drivers offer a rich function library that can be utilized in various application programs. This function library consists of numerous APIs that support many development tools, such as Visual Studio .NET, Visual C++, Visual Basic, Delphi and C++ Builder.

According to their functions or services, APIs can be categorized into several function groups:

- Analog Input Function Group
- Analog Output Function Group
- Digital Input/Output Function Group
- Counter Function Group
- Port Function Group (direct I/O)
- Event Function Group

For the usage and parameters of each function, please refer to the *Using DAQNavi SDK* chapter in the *DAQNavi SDK Manual*.

Troubleshooting DAQNavi Device Drivers Error

Driver functions will return a status code when they are called to perform a certain task for the application. When a function returns a code that is not zero, it means the function has failed to perform its designated function. To troubleshoot the Device Drivers error, you can pass the error, you can check the error code and error description within the Error Control of each function in the DAQNavi SDK Manual.

1.6 Accessories

Advantech offers a complete set of accessory products to support the PCIE-1813 card. These accessories include:

Wiring Cables

- **PCL-101100R-1E** 100-pin SCSI (ribbon type) shielded cable, 1m
- **PCL-101100R-2E** 100-pin SCSI (ribbon type) shielded cable, 2m

Wiring Boards

- **ADAM-39100-AE** 100-pin DIN-rail SCSI wiring board
- **PCLD-8813-AE** 100-pin DIN-rail SCSI wiring board with isolation

Chapter 2

Installation

This chapter provides a packing item checklist, proper instructions for unpacking, and step-by-step procedures for both driver and card installation.

- Unpacking
- Driver Installation
- Hardware Installation
- Device Setup and Configuration

2.1 Unpacking

After receiving your PCIE-1813 package, inspect the contents. The package should include the following items:

- PCIE-1813 card
- Companion DVD-ROM (Device Drivers included)
- Startup Manual

The PCIE-1813 card has certain electronic components vulnerable to electrostatic discharge (ESD). ESD can easily damage the integrated circuits and certain components if preventive measures are ignored.

Before removing the card from the anti-static plastic bag, you should take following precautions to ward off possible ESD damage:

- Touch the metal part of your computer chassis with your hand to discharge the static electricity accumulated on your body. Alternatively, one can also use a grounding strap.
- Touch the anti-static bag to a metal part of your computer chassis before opening the bag.
- Take hold of the card only by the metal bracket when removing it from the bag.

After taking out the card, you should first:

- Inspect the card for any possible signs of external damage (loose or damaged components, etc.). If the card is visibly damaged, please notify our service department or our local sales representative immediately. Do not install a damaged card into your system.

Also pay extra attention to the following to ensure a proper installation:

- Avoid physical contact with materials that could hold static electricity such as plastic, vinyl and styrofoam.
- Whenever you handle the card, grasp it only by its edges. DO NOT TOUCH the exposed metal pins of the connector or the electronic components.

Note! *Keep the anti-static bag for future use. You might need the original bag to store the card if you have to remove the card from a PC or transport it elsewhere.*

2.2 Driver Installation

We recommend you install the driver *before* you install the PCIE-1813 card into your system, since this will guarantee a smooth installation process.

The Advantech DAQNavi Device Drivers Setup program for the PCIE-1813 card is included in the companion DVD-ROM that is shipped with your DA&C card package. Please follow the steps below to install the driver software:

1. Insert the companion DVD-ROM into the DVD-ROM drive.
2. The Setup program should launch automatically if you have the autoplay function enabled on your system. When the Setup Program is launched, you will see the following Setup Screen.

Note! *If the autoplay function is not enabled on your computer, use Windows Explorer or Windows Run command to execute autorun.exe on the companion DVD-ROM.*

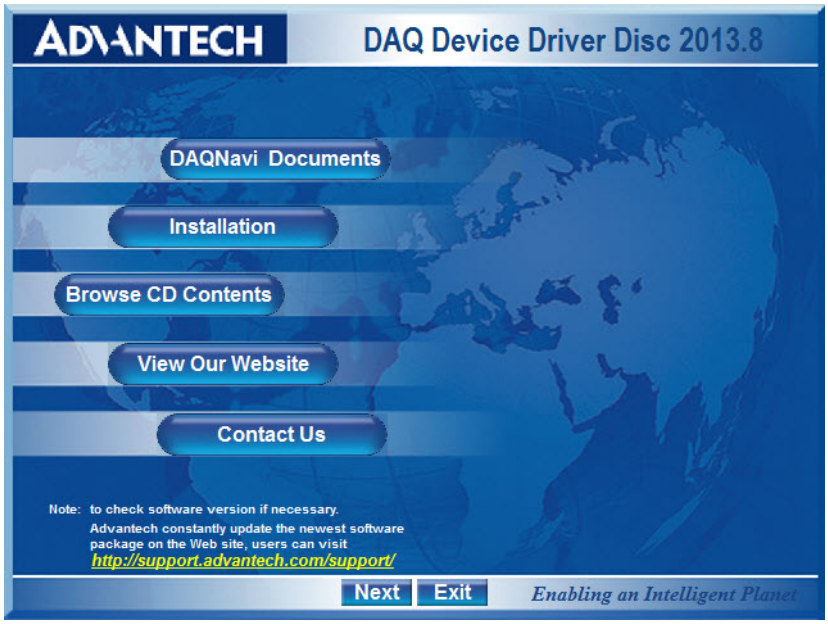


Figure 2.1 Advantech automation software setup screen

3. Select the Installation option.
4. Select the Legacy SDK and Drivers option to install.
5. Select the Individual Drivers option.
6. Select the PCIe series and the specific device then follow the installation instructions step by step to complete your device driver installation and setup.
7. Press the Back button and select the Windows SDK and Drivers and install the Advantech Navigator.

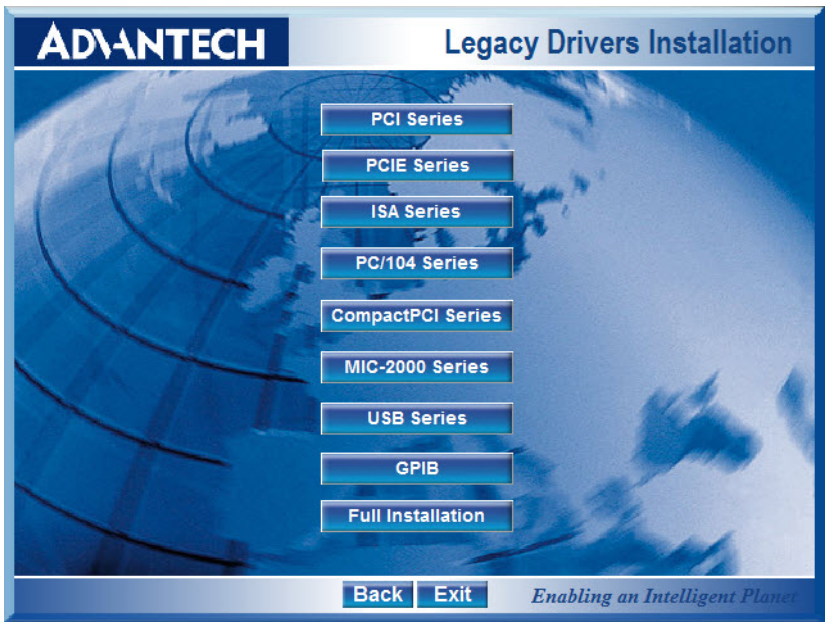


Figure 2.2 The various options for driver setup

For further information on driver-related issues, an online version of the *DAQNavi SDK Manual* is available by accessing the following path:

Start/Programs/Advantech Automation/DAQNavi/DAQNavi Manuals/DAQNavi SDK Manual

2.3 Hardware Installation

Note! *Make sure you have installed the driver first before you install the card (refer to 2.2 Driver Installation)*

After installing the device drivers, install the PCIE-1813 card in the computer. However, it is suggested that you refer to the computer's user manual or related documentation if you have any doubts. Please follow the steps below to install the card in your system.

1. Power off your computer and unplug the power cord and cables. Do this before installing or removing any components on the computer.
2. Remove the cover of your computer.
3. Remove the slot cover on the back panel of your computer.
4. Touch the metal part on the surface of your computer to neutralize any static electricity that might be on your body.
5. Insert the PCIE-1813 card into the PCI Express interface. Hold the card only by its edges and carefully align it with the slot. Insert the card firmly into place. Use of excessive force must be avoided; otherwise, the card might be damaged.
6. Connect appropriate accessories (100-pin SCSI shielded cable, wiring terminals, etc., if necessary) to the card.
7. Replace the cover of your computer chassis. Re-connect the cables you removed in step 1.
8. Plug in the power cord and turn on the computer.

After your card is properly installed on your system, you can now configure your device using the *Advantech Navigator* Program that has itself already been installed on your system during driver setup. A complete device installation procedure should include device setup, configuration and testing. The following sections will guide you through the Setup, Configuration and Testing of your device.

2.4 Device Setup and Configuration

The *Advantech Navigator* program is a utility that allows you to set up, configure and test your device, and later stores your settings on the system registry. These settings will be used when you call the APIs of Advantech Device Drivers. Take the following PCIE-1813 details as an example.

Setting Up the Device

1. To install the I/O device for your card, first run the *Advantech Navigator* program (by accessing *Start/Programs/Advantech Automation/Navigator for DN4*).
2. You can then view the device(s) already installed on your system (if any) in the Installed Devices list box. If the software and hardware installation are completed, you will see PCIE-1813 card in the Installed Devices list.

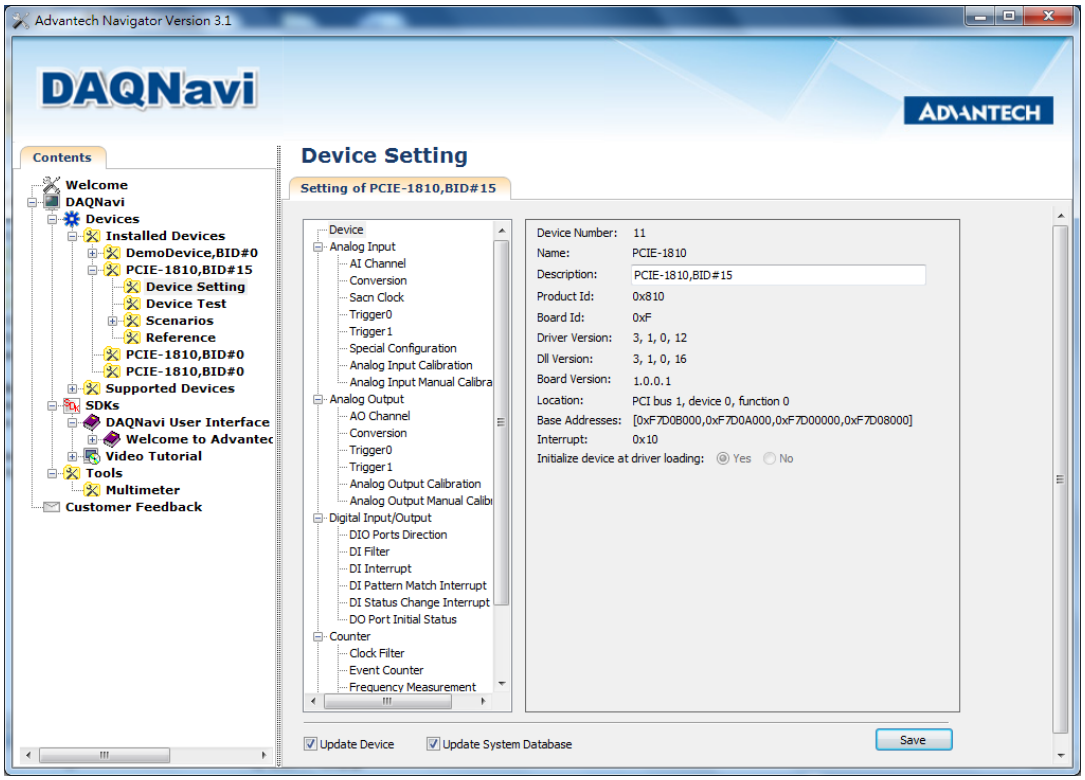


Figure 2.3 PCIE-1813 device settings

Configuring the Device

3. Go to Device Setting to configure your device. Here you can configure not only the Analog Input/Output of PCIE-1813 but also Digital Input/Output.

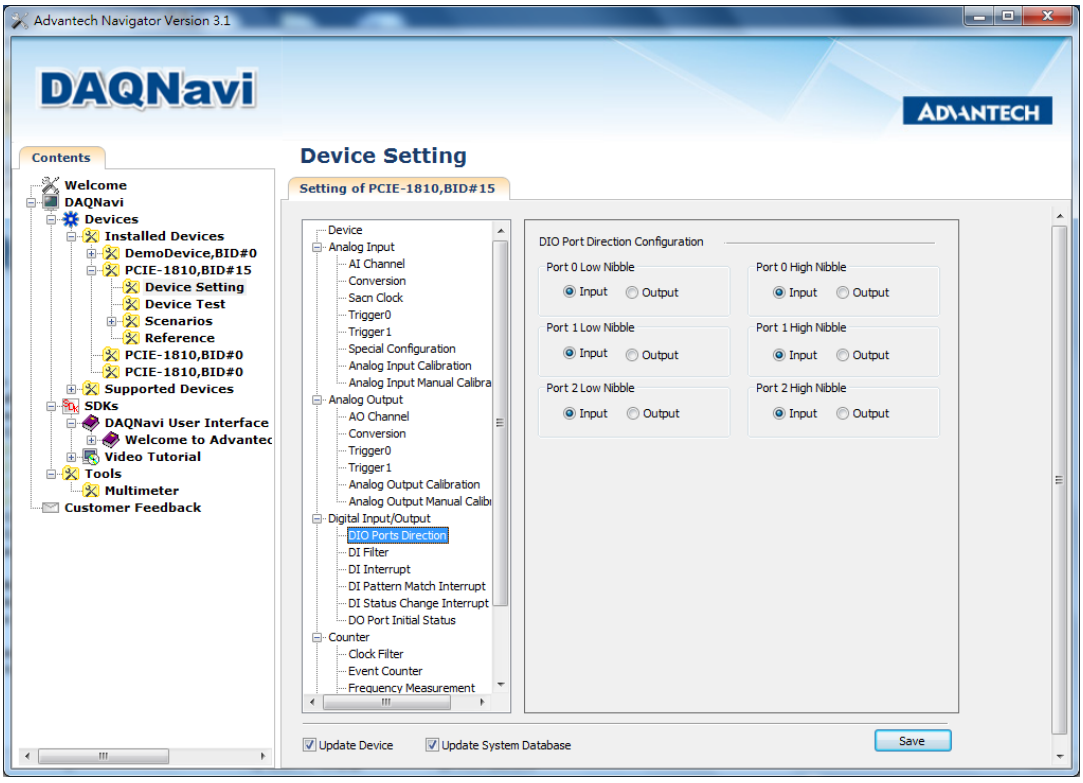


Figure 2.4 Device settings page

4. After your card is properly installed and configured, you can go to the *Device Test* page to test the hardware using the testing utility supplied.

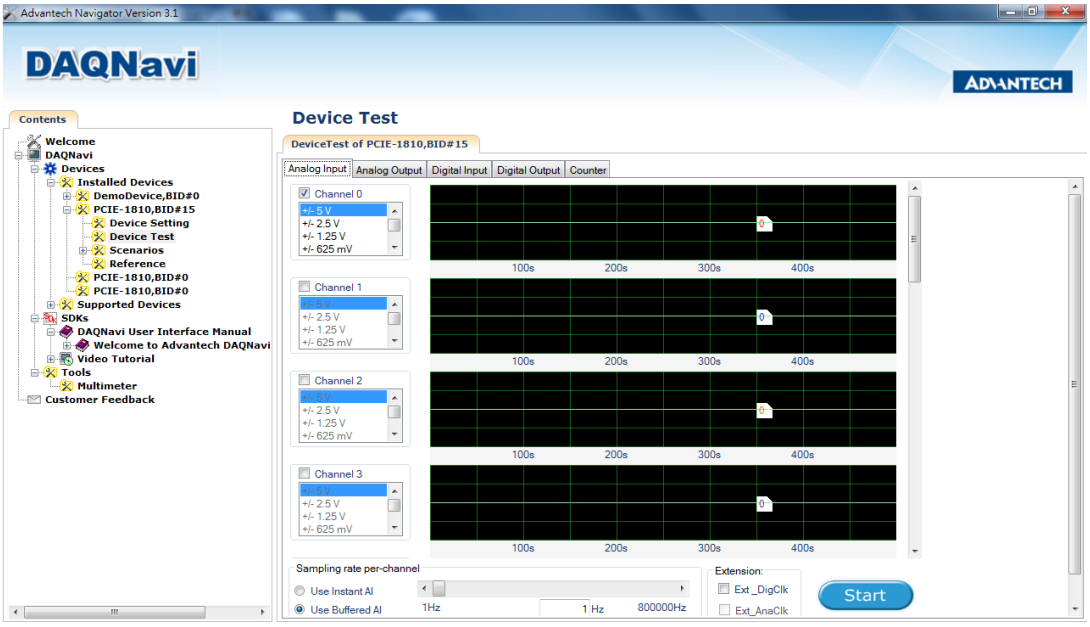


Figure 2.5 PCIE-1813 device testing

For more detailed information, please refer to the DAQNavi SDK manual or the user interface manual in the Advantech Navigator.

Chapter 3

Signal Connections

This chapter provides useful information about how to connect input and output signals to the PCIE-1813 card via the I/O connector.

- Overview
- Board ID Settings
- Signal Connections
- Analog Input
- Field Wiring Considerations

3.1 Overview

Maintaining signal connections is one of the most important factors in ensuring that your application system is sending and receiving data correctly. A good signal connection can avoid unnecessary and costly damage to your PC and other hardware devices. This chapter provides useful information about how to connect input and output signals to the PCIE-1813 card via the I/O connector.

3.2 Switch and Jumper Settings

Please refer to Figure 3.1 for jumper and switch locations on PCIE-1813.

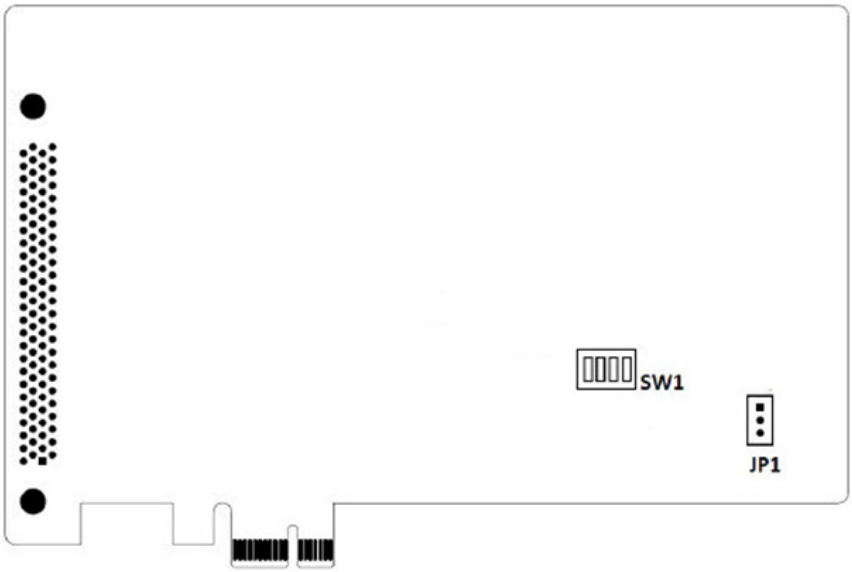


Figure 3.1 Connector and switch locations

3.2.1 Board ID (SW1)

The PCIE-1813 has a built-in DIP switch (SW1), which is used to define each card's board ID. When there are multiple cards on the same chassis, this board ID switch is used to set each card's device number.

After setting each PCIE-1813, you can identify each card in system with different device numbers. The default value of board ID is 0 and if you need to adjust it to other value, set the SW1 by referring to Table 3.1.

Table 3.1: Board ID Setting (SW1)

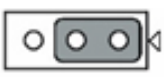
SW1	Position 1	Position 2	Position 3	Position 4
BoardID	Bit0	Bit1	Bit2	Bit3
0	ON	ON	ON	ON
1	ON	ON	ON	OFF
2	ON	ON	OFF	ON
3	ON	ON	OFF	OFF
4	ON	OFF	ON	OFF
5	ON	OFF	ON	OFF
6	ON	OFF	OFF	ON
7	ON	OFF	OFF	OFF
8	OFF	ON	ON	ON
9	OFF	ON	ON	OFF
10	OFF	ON	OFF	ON
11	OFF	ON	OFF	OFF
12	OFF	OFF	ON	ON
13	OFF	OFF	ON	OFF
14	OFF	OFF	OFF	ON
15	OFF	OFF	OFF	OFF

Default Setting is 0

3.2.2 Power On Configuration (JP1)

Default configuration after power on, and hardware reset is to set all the digital output and analog output channels to open status (output voltage equals zero) so that external devices will not be damaged when the system starts or resets. When the system is hot reset, then the status of isolated digital output channels are selected by jumper JP1. Table 3.2 shows the possible configurations of jumper JP1.

Table 3.2: Power on Configuration after Hot Reset (JP1)

JP1	Power on configuration after hot reset
1 	Keep same status as before reset
1 	Default configuration (DO status low)

3.3 Signal Connections

Pin Assignments

The I/O connector on the PCIE-1813 is a 100-pin connector that enables you to connect to accessories with the PCL-101100R shielded cable.

Figure 3.2 shows the pin assignments for the 100-pin I/O connector on PCIE-1813, and its I/O connector signal description.

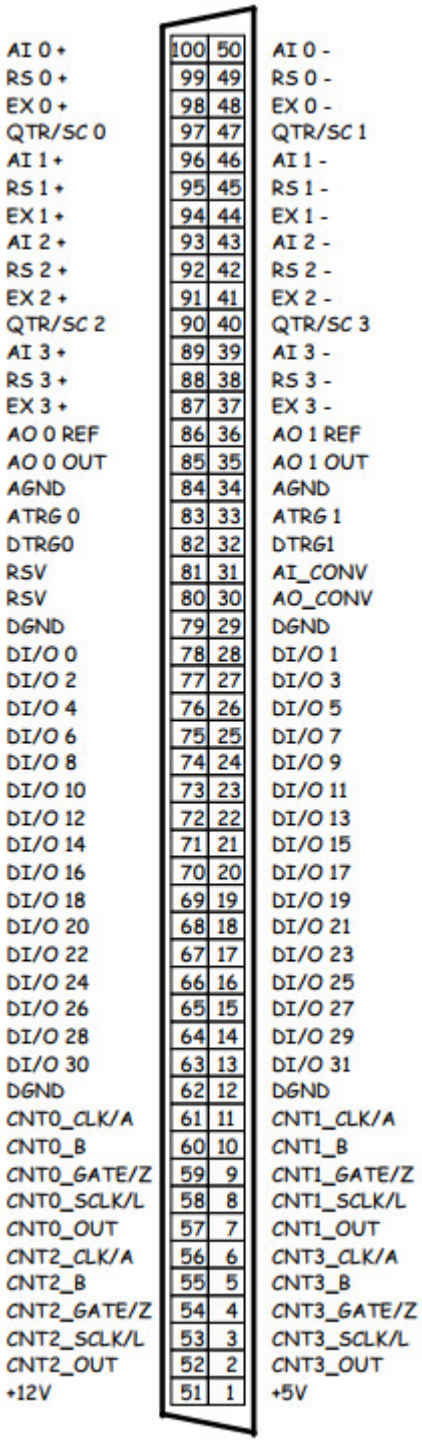


Figure 3.2 100-pin I/O connector pin assignments

3.3.1 I/O Connector Signal Description

Pin Name	Type	Pin#	Description
Analog Input			
AI0+	I	100	Positive terminal of analog input channel 0
AI0-	I	50	Negative terminal of analog input channel 0
RS0+	I	99	Positive remote sensing terminal of AI 0
RS0-	I	49	Negative remote sensing terminal of AI 0
EX0+	O	98	Positive excitation voltage terminal of AI 0
EX0-	O	48	Negative excitation voltage terminal of AI 0
QTR/SC0	-	97	Quarter bridge completion/shunt calibration terminal of AI 0
QTR/SC1	-	47	Quarter bridge completion/shunt calibration terminal of AI 1
AI1+	I	96	Positive terminal of analog input channel 1
AI1-	I	46	Negative terminal of analog input channel 1
RS1+	I	95	Positive remote sensing terminal of AI 1
RS1-	I	45	Negative remote sensing terminal of AI 1
EX1+	O	94	Positive excitation voltage terminal of AI 1
EX1-	O	44	Negative excitation voltage terminal of AI 1
AI2+	I	93	Positive terminal of analog input channel 2
AI2-	I	43	Negative terminal of analog input channel 2
RS2+	I	92	Positive remote sensing terminal of AI 2
RS2-	I	42	Negative remote sensing terminal of AI 2
EX2+	O	91	Positive excitation voltage terminal of AI 2
EX2-	O	41	Negative excitation voltage terminal of AI 2
QTR/SC2	-	90	Quarter bridge completion/shunt calibration terminal of AI 2
QTR/SC3	-	40	Quarter bridge completion/shunt calibration terminal of AI 3
AI3+	I	89	Positive terminal of analog input channel 3
AI3-	I	39	Negative terminal of analog input channel 3
RS3+	I	88	Positive remote sensing terminal of AI 3
RS3-	I	38	Negative remote sensing terminal of AI 3
EX3+	O	87	Positive excitation voltage terminal of AI 3
EX3-	O	37	Negative excitation voltage terminal of AI 3
Analog Output			
AO0_REF	I	86	External reference voltage input for analog output channel 0
AO0_OUT	O	85	Voltage output of analog output channel 0
AO1_REF	I	36	External reference voltage input for analog output channel 1
AO1_OUT	O	35	Voltage output of analog output channel 1
Timing Signals			
ATRG0	I	83	Analog threshold trigger input channel 0
ATRG1	I	33	Analog threshold trigger input channel 1
DTRG0	I	82	Digital trigger input channel 0
DTRG1	I	32	Digital trigger input channel 1
AI_CONV	I	31	External analog input conversion clock
AO_CONV	I	30	External analog output conversion clock
Digital Input/Output			
DIO0	I/O	78	Digital input/output channel 0

DIO1	I/O	28	Digital input/output channel 1
DIO2	I/O	77	Digital input/output channel 2
DIO3	I/O	27	Digital input/output channel 3
DIO4	I/O	76	Digital input/output channel 4
DIO5	I/O	26	Digital input/output channel 5
DIO6	I/O	75	Digital input/output channel 6
DIO7	I/O	25	Digital input/output channel 7
DIO8	I/O	74	Digital input/output channel 8
DIO9	I/O	24	Digital input/output channel 9
DIO10	I/O	73	Digital input/output channel 10
DIO11	I/O	23	Digital input/output channel 11
DIO12	I/O	72	Digital input/output channel 12
DIO13	I/O	22	Digital input/output channel 13
DIO14	I/O	71	Digital input/output channel 14
DIO15	I/O	21	Digital input/output channel 15
DIO16	I/O	70	Digital input/output channel 16
DIO17	I/O	20	Digital input/output channel 17
DIO18	I/O	69	Digital input/output channel 18
DIO19	I/O	19	Digital input/output channel 19
DIO20	I/O	68	Digital input/output channel 20
DIO21	I/O	18	Digital input/output channel 21
DIO22	I/O	67	Digital input/output channel 22
DIO23	I/O	17	Digital input/output channel 23
DIO24	I/O	66	Digital input/output channel 24
DIO25	I/O	16	Digital input/output channel 25
DIO26	I/O	65	Digital input/output channel 26
DIO27	I/O	15	Digital input/output channel 27
DIO28	I/O	64	Digital input/output channel 28
DIO29	I/O	14	Digital input/output channel 29
DIO30	I/O	63	Digital input/output channel 30
DIO31	I/O	13	Digital input/output channel 31
Counter			
CNT0_CLK/A	I	61	Clock input (general purpose counter) or signal A input (encoder counter) of counter channel 0
CNT0_ B	I	60	Signal B input (encoder counter) of counter channel 0
CNT0_GATE/Z	I	59	Gate input (general purpose counter) or signal Z input (encoder counter) of counter channel 0
CNT0_SCLK/L	I	58	Sample clock input (general purpose counter) or latch input (encoder counter) of counter channel 0
CNT0_OUT	O	57	Output of counter channel 0
CNT1_CLK/A	I	11	Clock input (general purpose counter) or signal A input (encoder counter) of counter channel 1
CNT1_B	I	10	Signal B input (encoder counter) of counter channel 1
CNT1_GATE/Z	I	9	Gate input (general purpose counter) or signal Z input (encoder counter) of counter channel 1
CNT1_SCLK/L	I	8	Sample clock input (general purpose counter) or latch input (encoder counter) of counter channel 1
CNT1_OUT	O	7	Output of counter channel 1

CNT2_CLK/A	I	56	Clock input (general purpose counter) or signal A input (encoder counter) of counter channel 2
CNT2_ B	I	55	Signal B input (encoder counter) of counter channel 2
CNT2_GATE/Z	I	54	Gate input (general purpose counter) or signal Z input (encoder counter) of counter channel 2
CNT2_SCLK/L	I	53	Sample clock input (general purpose counter) or latch input (encoder counter) of counter channel 2
CNT2_OUT	O	52	Output of counter channel 2
CNT3_CLK/A	I	6	Clock input (general purpose counter) or signal A input (encoder counter) of counter channel 3
CNT3_B	I	5	Signal B input (encoder counter) of counter channel 3
CNT3_GATE/Z	I	4	Gate input (general purpose counter) or signal Z input (encoder counter) of counter channel 3
CNT3_SCLK/L	I	3	Sample clock input (general purpose counter) or latch input (encoder counter) of counter channel 3
CNT3_OUT	O	2	Output of counter channel 3
Power and Ground			
AGND	-	34, 38, 40, 42, 45, 47, 49, 84	Analog ground. Reference for all analog signals.
DGND	-	12, 29, 62, 79	Digital ground. Reference for all digital signals.
+12V	-	51	+12 V power supply for external use
+5V	-	1	+5 V power supply for external use
Others			
RSV	-	80, 81	Reserved. Do not connect.

3.4 Analog Input

3.4.1 Analog Input Overview

The analog input function of the PCIE-1813 has 26-bit resolution and supports sample rates up to 38.4 kS/s.

You can configure all settings on every single channel basis in software. The channels support the following features:

- Voltage and ratio metric (mV/V) measurements.
- Connecting sensors of all bridge configurations, including quarter-, half-, and full-bridge.
- DC voltage excitation between 0.5 V and 10V.
- Programmatic system calibration.
- Analog and digital filtering to reject out-of-band signals.
- Remote sense of bridge excitation.

3.4.2 Connecting Signals

PCIE-1813 is adopted Wheatstone bridge, and this section discusses how to connect the signals of supported strain-gauge configuration types.

Wheatstone Bridge

Many sensors, including strain-gauges, load cells, pressure sensors, and torque sensors are based on the concept of a Wheatstone bridge. There are four elements, or legs, in a Wheatstone bridge. In general, these elements can be resistive or reactive, but in the majority of bridge based sensors, the elements are resistive. Most Wheatstone bridge based sensors use all four legs of the bridge as active sensing elements. However, common strain gauge configurations include one, two or four active sensing elements. Figure 1-1 shows a resistive Wheatstone bridge circuit diagram.

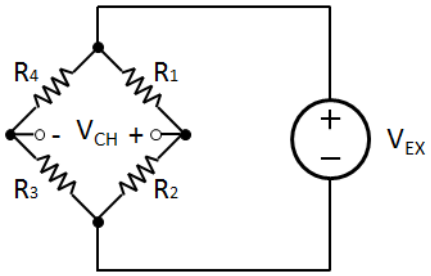


Figure 3.3 Basic Wheatstone bridge circuit diagram

The Wheatstone bridge is the electrical equivalent of two parallel voltage divider circuits. R1 and R2 compose one voltage divider circuit, and R4 and R3 compose the second voltage divider circuit. The output of a Wheatstone bridge is measured between the middle nodes of the two voltage dividers. A physical phenomena, such as a change in strain or temperature applied to a specimen, changes the resistance of the sensing elements in the Wheatstone bridge, resulting in a bridge output voltage that is proportional to the physical phenomena. The output voltage of the bridge scales with the excitation voltage. However, the ratio of the bridge output (VCH) and the excitation voltage (VEX) remains fixed over variations in excitation voltage, and it is this unitless ratio (VCH/VEX) that is of interest. To accurately measure the ratiometric output of a bridge based sensor, both the bridge output voltage (VCH) and the excitation voltage (VEX) must be known. Determination of the excitation voltage can be accomplished by either using an accurate voltage source or by measuring it. The PCIE-1813 uses circuitry that continuously measures the excitation voltage and plies it as a reference to its analog-to-digital converter (ADC). In this way the PCIE-1813 compensates for variations in the excitation voltage, and the card returns data as a ratio of the bridge output voltage to the excitation voltage.

3.4.3 Strain Gauge Sensor Configurations

This section describes the configurations and signal connection of various supported strain-gauge configuration types.

Quarter-Bridge Type I

This section provides information for the quarter-bridge strain-gauge configuration type I. The quarter-bridge type I measures either axial or bending strain. Figure 3.4 shows how to position a strain-gauge resistor in axial and bending configurations. Figure 3.5 shows the quarter-bridge type I circuit wiring diagram.

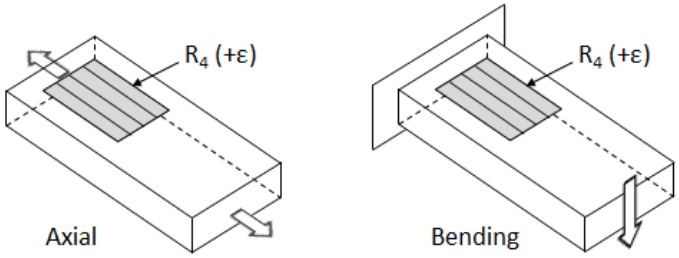


Figure 3.4 Quarter-bridge type I measuring axial and bending strain

A quarter-bridge type I configuration has the following characteristics:

- A single active strain-gauge element is mounted in the principal direction of axial or bending strain
- A passive quarter-bridge completion resistor (R3) is required in addition to half-bridge completion resistors (R1 and R2). These resistors are provided by the PCIE-1813.
- The shunt calibration resistor (RSC) and switch are provided by the PCIE-1813.
- Sensitivity ≈ 0.5 μV/V per με, for GF = 2.0.

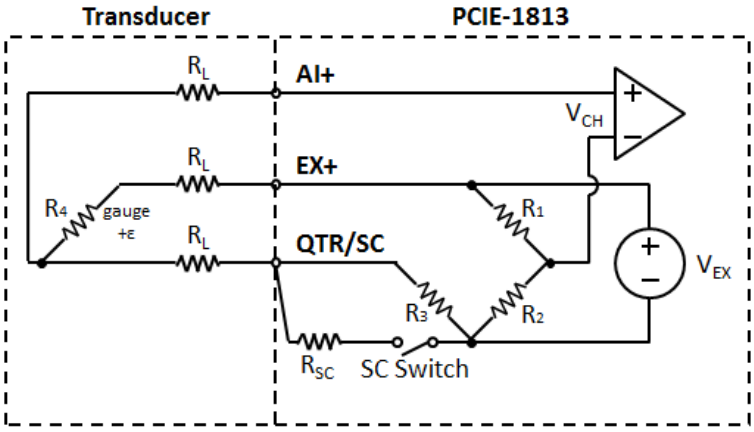


Figure 3.5 Quarter-bridge type I circuit diagram

Quarter-Bridge Type II

This section provides information for the quarter-bridge strain-gauge configuration type II. The quarter-bridge type II configuration measures either axial or bending strain. Figure 3.6 shows how to position a strain-gauge resistor in axial and bending configurations. Figure 3.7 shows the quarter-bridge type II circuit wiring diagram.

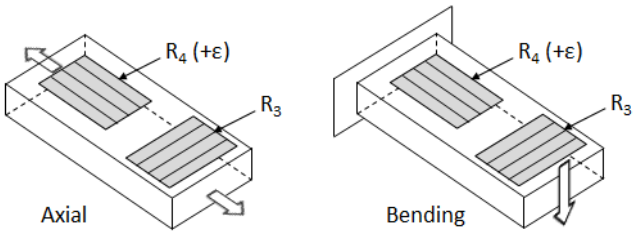


Figure 3.6 Quarter-bridge type II measuring axial and bending strain

A quarter-bridge type II configuration has the following characteristics:

- One active strain-gauge element and one passive quarter-bridge element (dummy gauge) used for temperature compensation. The active element (R4) is mounted in the direction of axial or bending strain. The dummy gauge (R3) is mounted in close thermal contact with the strain specimen but not bonded to the specimen, and is usually mounted perpendicular to the principal axis of strain.
- Completion resistors (R1 and R2) provide half-bridge completion. These resistors are provided by the PCIE-1813.
- Sensitivity ≈ 0.5 μV/V per με, for GF = 2.0.

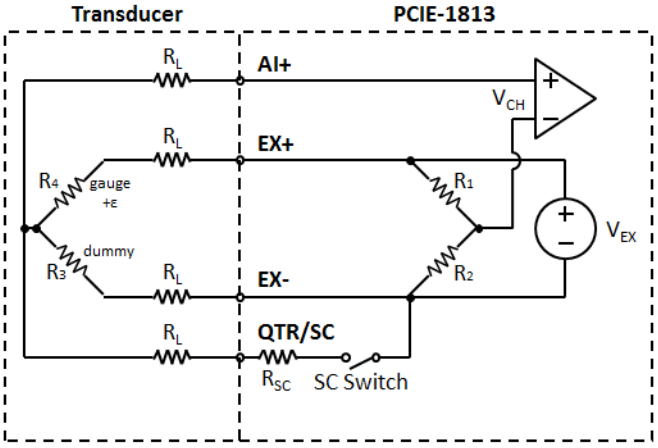


Figure 3.7 Quarter-bridge type I circuit diagram

Half-Bridge Type I

This section provides information for the half-bridge strain-gauge configuration type I. The half-bridge type I configuration measures either axial or bending strain. Figure 3.8 shows how to position a strain-gauge resistor in axial and bending configurations. Figure 3.9 shows the quarter-bridge type II circuit wiring diagram.

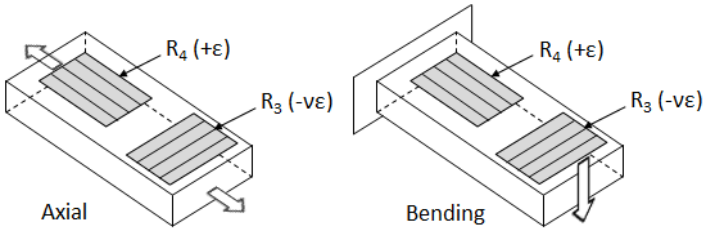


Figure 3.8 Half-bridge type I measuring axial and bending strain

A half-bridge type I configuration has the following characteristics:

- Two active strain-gauge elements. One strain-gauge element is mounted in the direction of axial strain while the other acts as a Poisson gauge and is mounted perpendicular to the principal axis of strain.
- Half-bridge completion resistors (R1 and R2) are provided by the PCIE-1813.
- Sensitive to both axial and bending strain.
- Sensitivity ≈ 0.65 μV/V per με, for GF = 2.0.

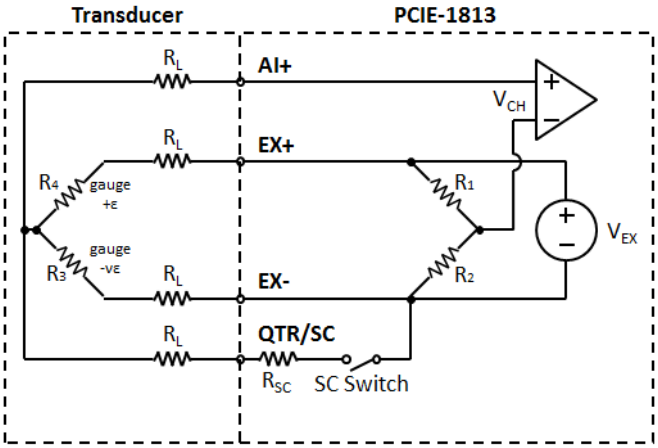


Figure 3.9 Half-bridge type I circuit diagram

Half-Bridge Type II

This section provides information for the half-bridge strain-gauge configuration type II. The half-bridge type II only measures bending strain. Figure 3.10 shows how to position strain-gauge resistors in a bending configuration. Figure 3.11 shows the half-bridge type II circuit wiring diagram.

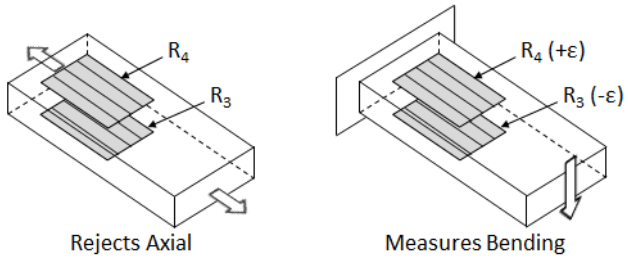


Figure 3.10 Half-bridge type II rejecting axial and measuring bending strain

A half-bridge type II configuration has the following characteristics:

- Two active strain-gauge elements. One strain-gauge element is mounted in the direction of bending strain on one side of the strain specimen (top) while the other is mounted in the direction of bending strain on the opposite side (bottom).
- Half-bridge completion resistors (R1 and R2) are provided by the PCIE-1813.
- Sensitive to bending strain.
- Rejects axial strain.
- Sensitivity ≈ 1 μV/V per με, for GF = 2.0.

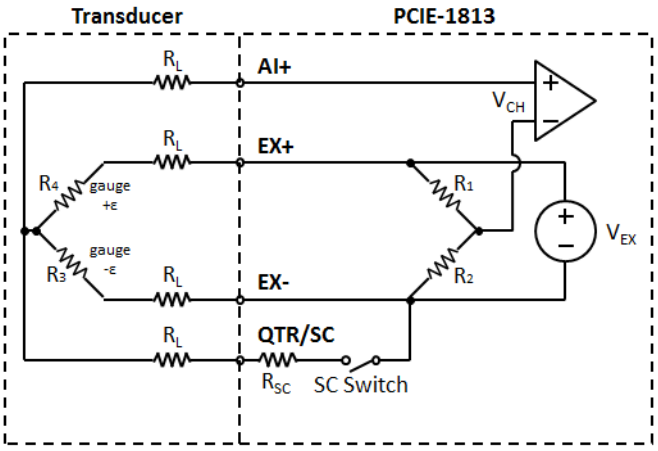


Figure 3.11 Half-bridge type II circuit diagram

Full-Bridge Type I

This section provides information for the full-bridge strain-gauge configuration type I. The full-bridge type I only measures bending strain. Figure 3.12 shows how to position strain-gauge resistors in a bending configuration. Figure 3.13 show the full-bridge type I circuit wiring diagram.

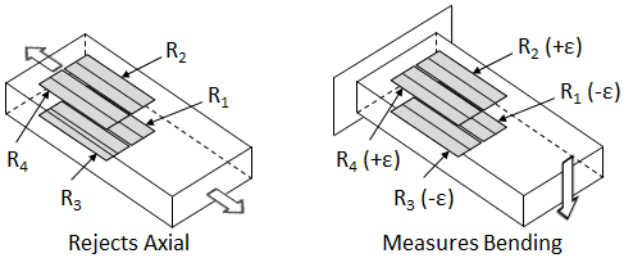


Figure 3.12 Full-bridge type I rejecting axial and measuring bending strain

A full-bridge type I configuration has the following characteristics:

- Four active strain-gauge elements. Two strain-gauge elements are mounted in the direction of bending strain on one side of the strain specimen (top) while the other two are mounted in the direction of bending strain on the opposite side (bottom).
- Highly sensitive to bending strain.
- Rejects axial strain.
- Sensitivity ≈ 2 μV/V per με, for GF = 2.0.

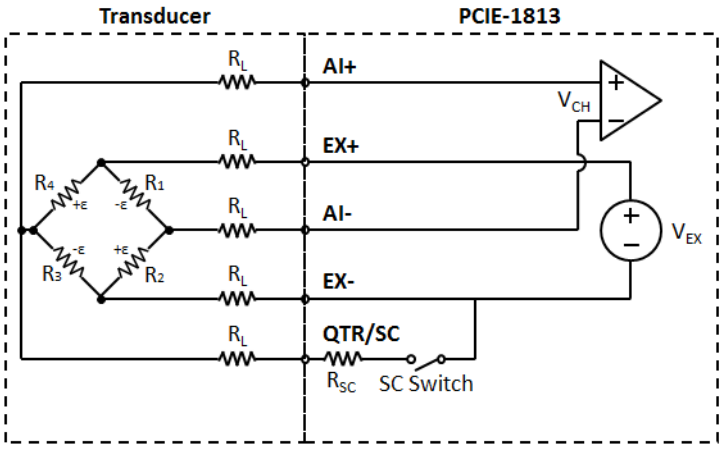


Figure 3.13 Full-bridge type I circuit diagram

Full-Bridge Type II

This section provides information for the full-bridge strain-gauge configuration type II. The full-bridge type II only measures bending strain. Figure 3.14 shows how to position strain-gauge resistors in a bending configuration. Figure 3.15 show the full-bridge type II circuit wiring diagram.

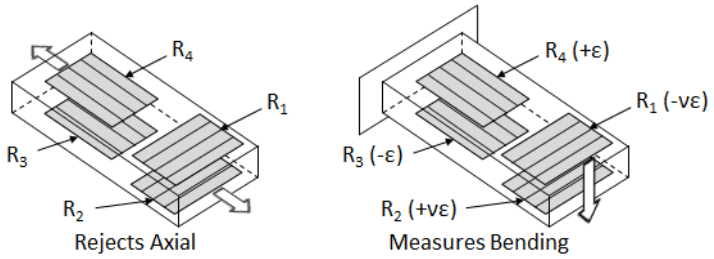


Figure 3.14 Full-bridge type II rejecting axial and measuring bending strain

A full-bridge type II configuration has the following characteristics:

- Four active strain-gauge elements. Two strain-gauge elements are mounted in the direction of bending strain with one on one side of the strain specimen (top) and the other on the opposite side (bottom). The other two act together as a Poisson gauge and are mounted transverse (perpendicular) to the principal axis of strain with one on one side of the strain specimen (top) and the other on the opposite side (bottom).
- Sensitive to bending strain.
- Rejects axial strain.
- Sensitivity ≈ 1.3 μV/V per με, for GF = 2.0.

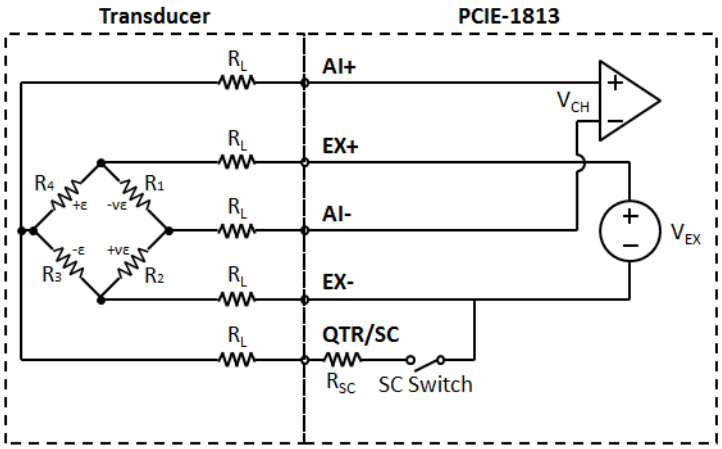


Figure 3.15 Full-bridge type II circuit diagram

Full-Bridge Type III

This section provides information for the full-bridge strain-gauge configuration type III. The full-bridge type III only measures axial strain. Figure 3.16 shows how to position strain-gauge resistors in a bending configuration. Figure 3.17 show the full-bridge type III circuit wiring diagram.

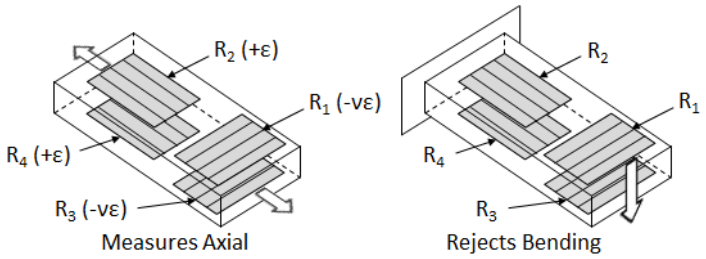


Figure 3.16 Full-bridge type III rejecting axial and measuring bending strain

A full-bridge type III configuration has the following characteristics:

- Four active strain-gauge elements. Two strain-gauge elements are mounted in the direction of axial strain with one on one side of the strain specimen (top) and the other on the opposite side (bottom). The other two act together as a Poisson gauge and are mounted transverse (perpendicular) to the principal axis of strain with one on one side of the strain specimen (top) and the other on the opposite side (bottom).
- Sensitive to axial strain.
- Rejects bending strain.
- Sensitivity ≈ 1.3 μV/V per με, for GF = 2.0.

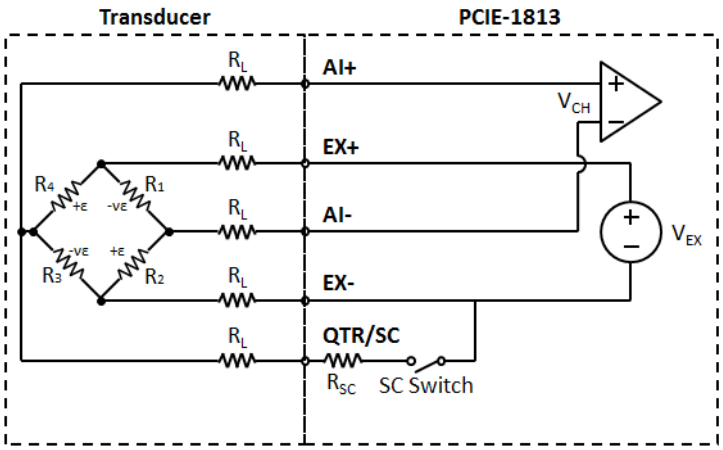


Figure 3.17 Full-bridge type III circuit diagram

Force, Pressure, and Torque Sensor Configurations

The PCIE-1813 can be used with force sensors (such as load cells), pressure sensors, or torque sensors that have the following characteristics:

- Wheatstone bridge based (Note 1)
- Unamplified mV/V or V/V output (Note 2)

These sensors typically use a full-bridge configuration with a 350 Ω nominal bridge resistance, but other configurations and nominal bridge resistances can be used. Figure 3.18 shows the force, pressure, torque sensor circuit diagram.

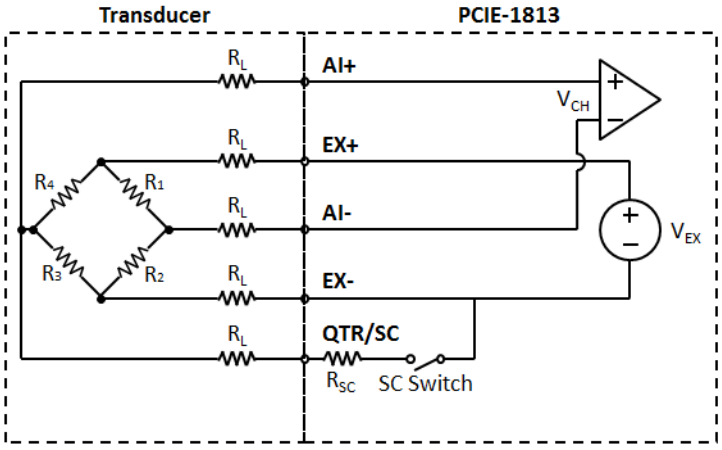


Figure 3.18 Full-bridge type III circuit diagram

AI Sample Clock Sources Connections

Internal AI Sample Clock

The internal AI sample clock uses a 100 MHz time base. Conversions start on the rising edge of the counter output. You can use software to specify the clock source as internal and the sampling frequency to pace the operation. The minimum frequency is 0.024 S/s, the maximum frequency is 38.4 KS/s. According to the sampling theory (Nyquist Theorem), you must specify a frequency that is at least twice as fast as the input's highest frequency component to achieve a valid sampling. For example, to accurately sample a 20 kHz signal, you have to specify a sampling frequency of at least 40 kHz. This consideration can avoid an error condition often know as aliasing, in which high frequency input components appear erroneously as lower frequencies when sampling.

External AI Sample Clock

The external AI sample clock is useful when you want to pace acquisitions at rates not available with the internal AI sample clock, or when you want to pace at uneven intervals. Connect an external AI sample clock to screw terminal AI_CLK on the screw terminal board. Conversions will start on the rising edge of the external AI sample clock input signal. You can use software to specify the clock source as external. The sampling frequency is always limited to a maximum of 38.4KHz for the external AI sample clock input signal.

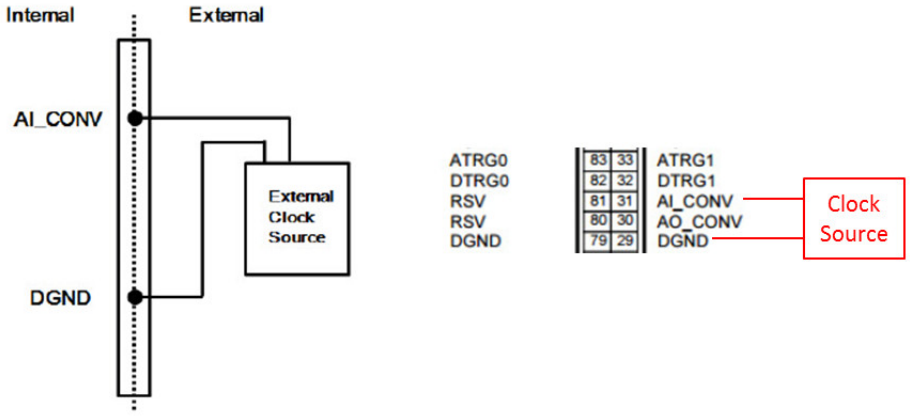


Figure 3.19 External clock source connection

Trigger Sources Connections

External Digital (TTL) Trigger

For analog input operations, an external digital trigger event occurs when the PCIE-1813 detects either a rising or falling edge on the External AI TTL trigger input signal from screw terminal DTRG0 and DTRG1 on the screw terminal board. The trigger signal is TTL-compatible.

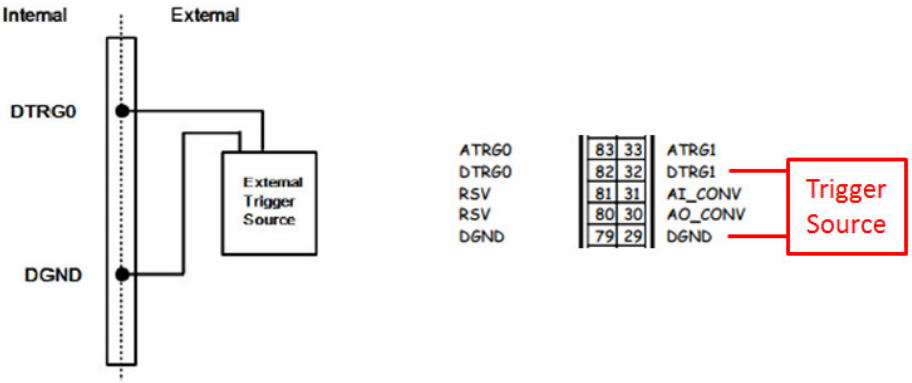


Figure 3.20 External digital trigger source connection

Analog Threshold Trigger

For analog input operations, an analog trigger event occurs when the PCIE-1813 detects a transition from above a threshold level to below a threshold level (falling edge), or a transition from below a threshold level to above a threshold level (rising edge). User should connect analog signal from an external device or analog output channel on board to external input signal ATRG0 and ATRG1. On the PCIE-1813, the threshold level is set using a dedicated 16-bit DAC. By software, you can program the threshold level by writing a voltage value to this DAC; this value can range from -10V to +10V.

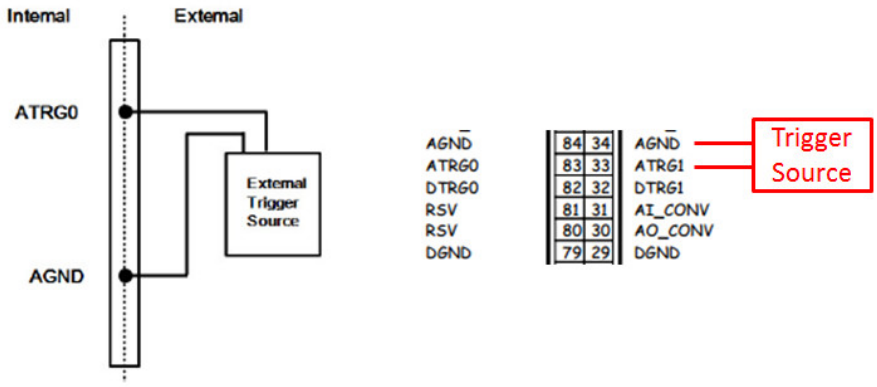


Figure 3.21 External analog trigger source connection

Analog Output Connection

The PCIE-1813 provides two AO output channels. You can use the internal precision -5 V or -10 V reference to generate 0 to +5 V or 0 to +10 V AO output. Use an external reference for other AO output ranges. The maximum reference input voltage is ±10 V and maximum output scaling is ±10 V. Loading current for AO outputs should not exceed 5 mA.

Figure 3.8 shows how to make analog output and external reference input connections on the PCIE-1813.

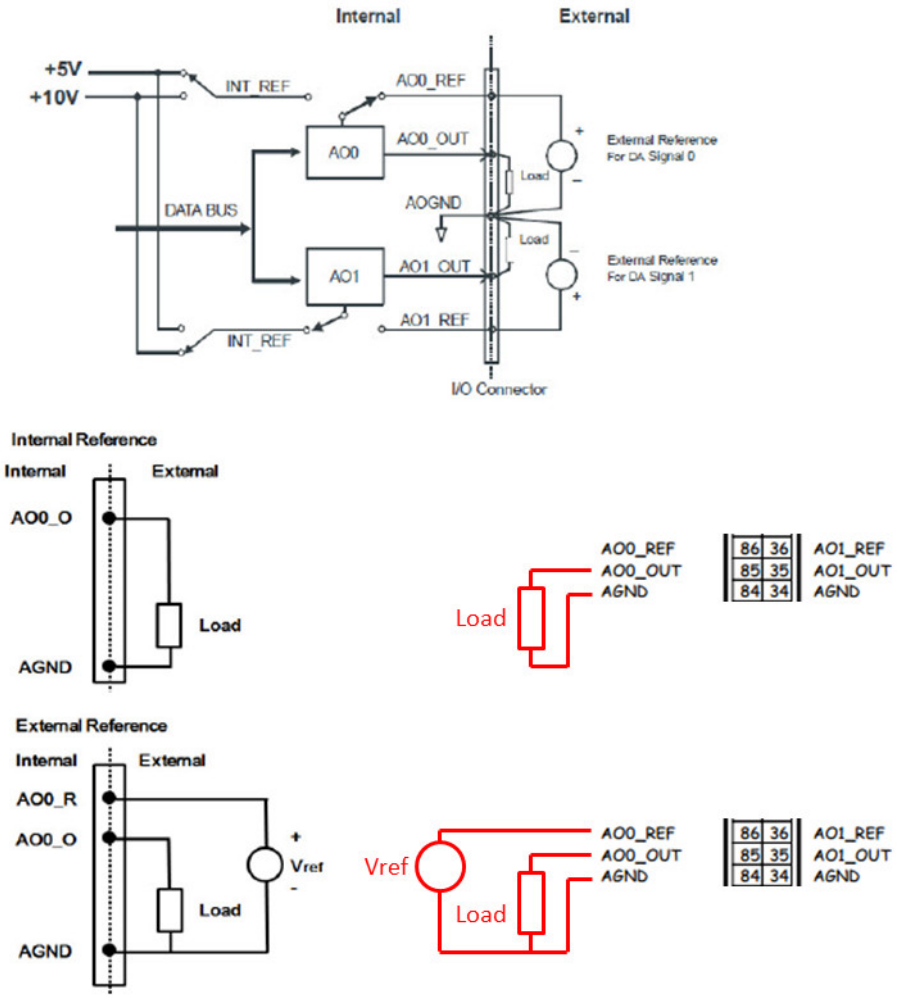


Figure 3.22 Analog output connections

AO Sample Clock Sources Connections

Internal AO Output Clock

The internal AO output clock applies a 100MHz time base divided by a 32-bit counter. Conversions start on the rising edges of counter output. Through software, user can specify the clock source and clock frequency to pace the analog output operation. The maximum frequency is 3.030303MS/s.

External AO Output Clock

The external AO output clock is useful when you want to pace analog output operations at rates not available with the internal AO output clock, or when you want to pace at uneven intervals. Connect an external AO output clock to the pin and then the conversions will start on input signal's rising edge. You can use software to specify the clock source as external. The maximum input clock frequency is 3MS/s.

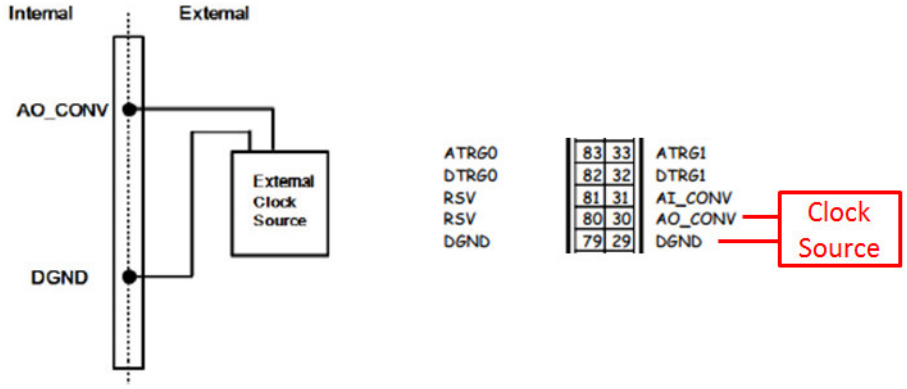


Figure 3.23 External clock source connection

Trigger Sources Connections

External Digital (TTL) Trigger

The PCIE-1813 supports external digital (TTL) trigger to activate AO conversions for continuous output mode. An external digital trigger event occurs when the PCIE-1813 detects either a rising or falling edge on the External AO TTL trigger input signal from the pin of connector. User can define the type of trigger source as rising-edge or falling-edge by software. The trigger signal is TTL-compatible.

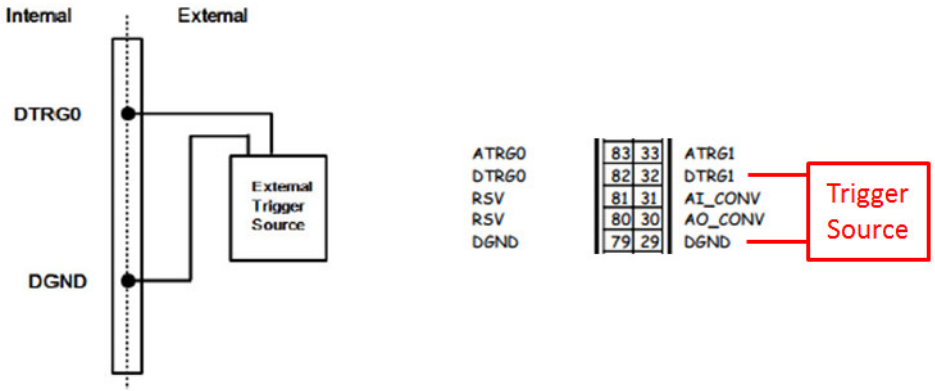


Figure 3.24 External digital trigger source connection

3.4.4 Digital Signal Connections

The PCIE-1813 has 32 digital input/output channels and they can be configured as input or output channels. The digital I/O levels are TTL compatible.

Digital Input Connections

Each digital input channel accepts either dry contact or 0 ~ 5 V_{DC} wet contact inputs. Dry contact capability allows the channel to respond to change in external circuit when no voltage exists.

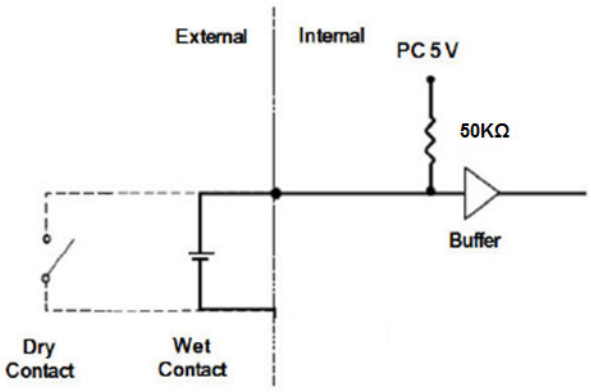


Figure 3.25 Wet and dry contacts

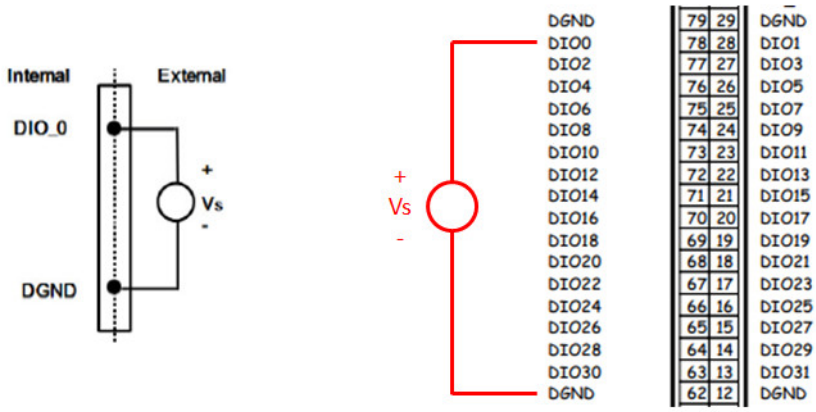


Figure 3.26 Digital input wet signal connection

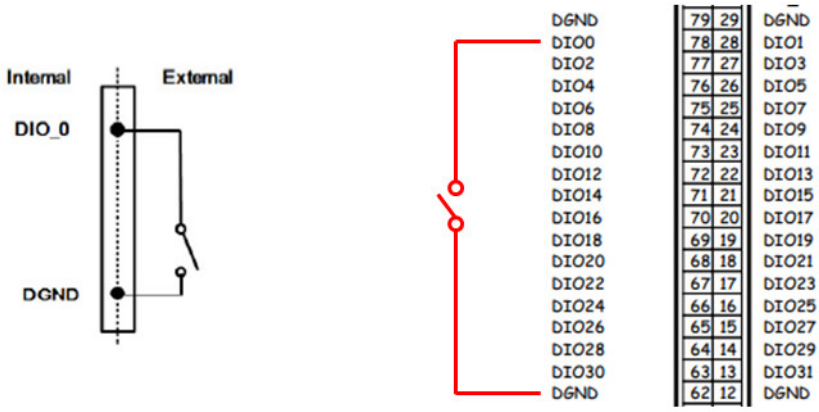


Figure 3.27 Digital input dry signal connection

Digital Output Connections

PCIE-1813 also has TTL digital output.

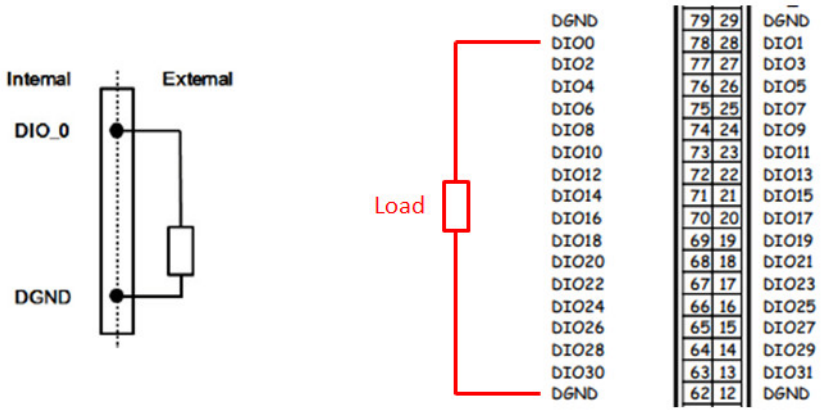


Figure 3.28 Digital output channel connections

3.5 Field Wiring Considerations

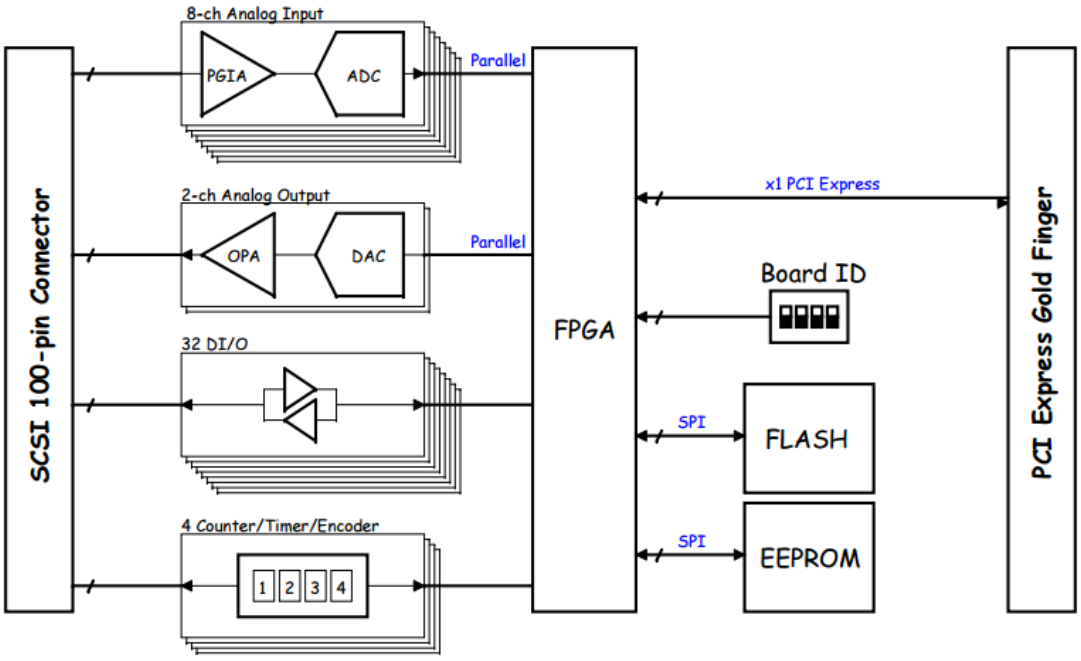
When you use PCIE-1813 cards to acquire data from outside, noises in the environment might significantly affect the accuracy of your measurements if due cautions are not taken. The following measures will be helpful to reduce possible interference running signal wires between signal sources and the PCIE-1813 card.

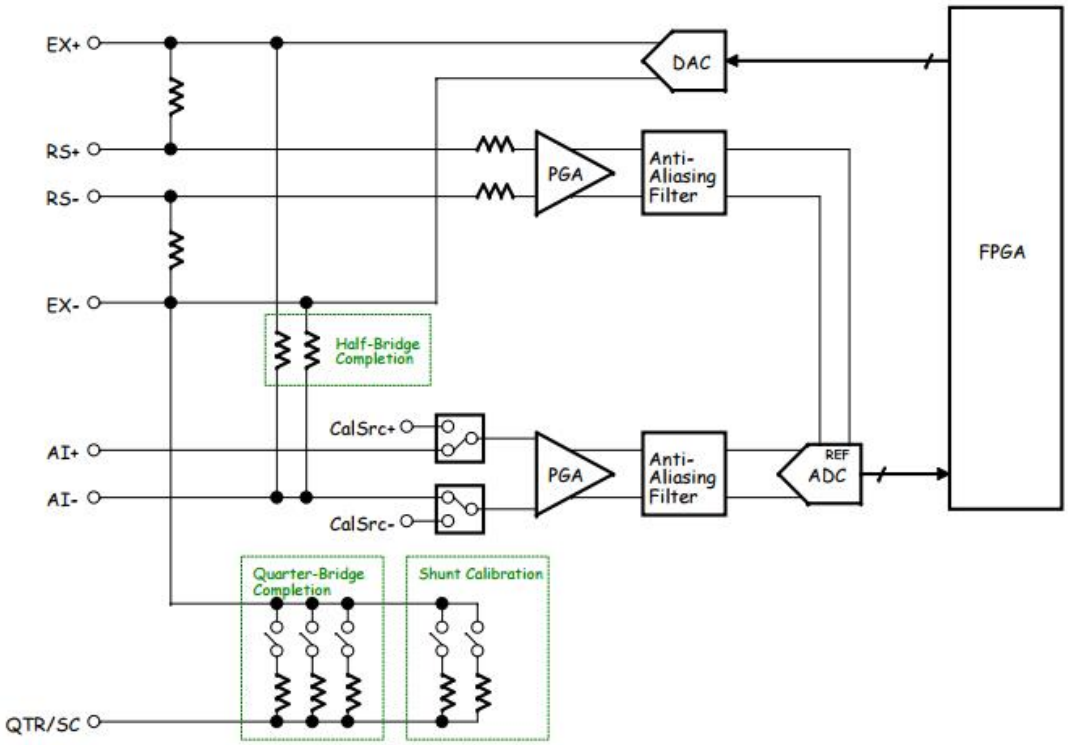
- The signal cables must be kept away from strong electromagnetic sources such as power lines, large electric motors, circuit breakers or welding machines, since they may cause strong electromagnetic interference. Keep the analog signal cables away from any video monitor, since it can significantly affect a data acquisition system.
- If the cable travels through an area with significant electromagnetic interference, you should adopt individually shielded, twisted-pair wires as the analog input cable. This type of cable has its signal wires twisted together and shielded with a metal mesh. The metal mesh should only be connected to one point at the signal source ground.
- Avoid running the signal cables through any conduit that might have power lines in it.
- If you have to place your signal cable parallel to a power line that has a high voltage or high current running through it, try to keep a safe distance between them. Alternatively, you can place the signal cable at a right angle to the power line to minimize the undesirable effect.
- The signals transmitted on the cable will be directly affected by the quality of the cable. In order to ensure better signal quality, we recommend that you use PCL-101100R shielded cable.

Appendix A

Specifications

A.1 Function Block





A.2 Analog Input

Channels		4 differential, can be enabled/disabled for each channel						
Resolution		26-bit						
Build-in memory		1K samples						
Sampling Rate		38.4 KS/s for each channel						
Voltage Input								
Input range		Bipolar	±10	±5	±2.5	±1.25	±0.625	± 0.3125
Absolute accuracy		Offset error	±0.1 mV					
		Gain error	±0.01% of full-scale range					
Temperature drift		Offset	25 ppm/ °C					
		Gain	15 ppm/ °C					
Input Impedance		1GΩ / 350pF						
Bridge Input								
Input Range (V)		±1 V/V	±500 mV/V	±250 mV/V	±125 mV/V	±62.5 mV/V	±31.25 mV/V	
Bridge completion		Full, half, quarter						
Half-bridge	Tolerance	±500 µV/V max.						
	Stability	2.5 µV/V per °C max.						
Quarter-bridge completion	Values	120 Ω, 350 Ω, 1 kΩ						
	Tolerance	±0.1% max.						
	Stability	10 ppm/ °C max.						
Shunt Calibration	Values	33.333 kΩ, 50 kΩ, 100 kΩ						
	Tolerance	±0.1% max.						
	Stability	10 ppm/ °C max.						
Excitation characteristics	Values	120 Ω bridge: 0 ~ +3 V						
		350 Ω bridge: 0 ~ +10 V						
		1 kΩ bridge: 0 ~ +10 V						
	Tolerance	±2% max.						
Accuracy	Offset error	±0.1 mV						
	Gain error	±0.15% of full-scale range						
Drift	Offset drift	25 ppm/ °C						
	Gain drift	15 ppm/ °C						

A.3 Analog Output

Channels	2	
Resolution	16-bit	
Memory Size	8K samples	
Update Rate	3 MS/s	
Output Range	Internal Reference	0V~5V, 0V~10V, ±5V, ±10V
	External Reference	0V~xV, -xV~+xV (10 ≤ x ≤ 10)
Accuracy	Relative	±1 LSB
	Differential Non-Linearity	±1 LSB (monotonic)
Slew Rate	20 V/us	
Gain Error	Adjustable to zero	
Drift	30 ppm/ ˚C	
Driving Capability	5 mA	
Update Mode	static update, waveform	
Output Impedance	max. 0.1 Ω	

A.4 Digital Input/Output

Channels	32 (shared)	
Input Voltage	Low	1.5 V max.
	High	3.5 V min.
Output Voltage	Low	0.5 V max.@ +20 mA (sink)
	High	4.5 V min.@ -20 mA (source)
Input Load	50KΩ pull-high resistor connect to 5V	
Digital Input Filter	1.28 us, 10.24 us, 163.84 us, or 1.31 ms (Each channel individually enable/disable)	
Interrupt	DI interrupt (rising, falling, or both edge), DI status change detect, DI pattern match detect (4 ports independently)	

A.5 Counter/Timer

Channels	4 channels (independent)	
Resolution	32-bit	
Digital Input Filter	1.28 us, 10.24 us, 163.84 us, or 1.31 ms (Each channel individually enable/disable)	
Counter Measurements	Event counting, frequency measurement, pulse width measurement	
Position Measurements	Quadrature encoding (X1, X2, and X4; Channel Z reload), two pulse encoding, signed pulse encoding	
Output Applications	One shot, timer/pulse, pulse width modulation, position comparison	
Compatibility *	TTL level	
Base Clock	Internal 20MHz or external clock (10 MHz max.). Selected by software	
Output Frequency	Max. 10MHz	
Clock Input	Low	1.5 V max.
	High	3.5 V min.
Gate Input	Low	1.5 V max.
	High	3.5 V min.
Counter Output	Low	0.5 V max. @+15mA
	High	4.5 V min. @-15mA
Error in Advanced Functions	Frequency Measurement	0.1% when input signal frequency ≥ 20KHz
	Pulse Width Measurement	0.1% when input signal frequency ≥ 20KHz
	Pulse Output	within 2% when output frequency > 20Hz
	PWM Output	within 2% when output frequency > 20Hz

* PCIE-1813 only supports single-ended signal. For differential line driver output encoders, a PCLD-8813 signal conditioning board is required.

Note! *When performing advanced functions, like frequency measurement and pulse output, there will be errors. And the error will vary depending on the parameter selections and the OS performance.*

A.6 General

I/O Connector Type	100-pin SCSI female	
Dimensions	167 x 100 mm (6.57 x 3.93 in)	
Power Consumption	Typical	3.3 V @ 200 mA, 12 V @ 310 mA
	Max.	3.3 V @ 450 mA, 12 V @ 650 mA
Temperature	Operating	0 ~ 6 0 °C (32 ~ 140 °F)
	Storage	-40 ~ 70 °C (-40 ~ 158 °F)
Relative Humidity	Operating	5~85%RH non-condensing
	Storage	5~95%RH non-condensing
Certifications	CE/FCC certified	

Appendix B

Operation Theory

B.1 Analog Input Operation

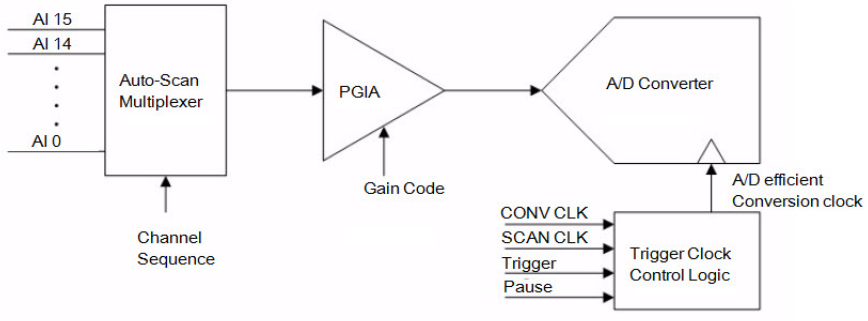
This section describes the following features of analog input operation theory that can help you realize how to configure the functions and parameters to match various applications.

- AI Hardware Structure
- Analog input ranges and gains
- Analog data acquisition mechanism
- Analog input acquisition modes
- AI CONV clock source
- AI trigger sources
- Analog input data format

B.1.1 AI Hardware Structure

The AI conversion hardware structure includes four major parts:

- **PGIA** (Programmable Gain Instrument Amplifier) rectifies the input range and amplify/alleviate input signal to match the input range of A/ D converter.
- **AI converter** conceives the rectified voltage from PGIA and transfers it into the corresponding digital data format.
- **Trigger/Clock control logic** enables/disables the whole process and determines acquisition timing interval.



AI Conversion Hardware Structure

B.1.2 Analog Input Ranges and Gains

The PCIE-1813 can measure bipolar analog input signals. A bipolar signal can range from 0 to ±10 V FSR (Full Scale Range). The PCIE-1813 provides various programmable gain levels and each channel is allowed to set its own input range individually. Table B.1 lists the effective ranges supported by the PCIE-1813 with gains.

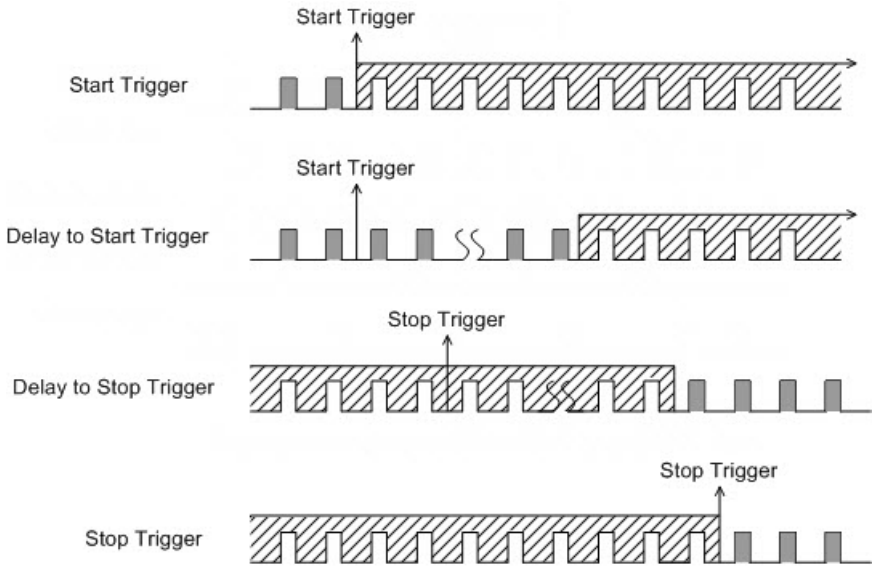
Table B.1: Gains and Analog Input Range

Bipolar Analog Input Range
±10 V
±5 V
±2.5 V
±1.25 V
±0.625 V
±0.3125 V

For each channel, choose the gain level providing the most optimal range that can accommodate the signal range you want to measure.

B.1.3 AI Trigger Modes

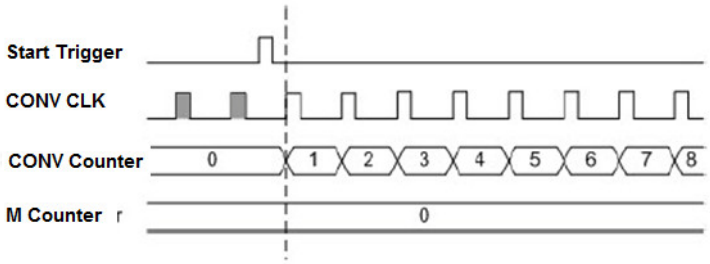
The PCIE-1813 supports four trigger modes and pause function. User can start or stop the operation by trigger mode selection. An extra 24-bit counter is dedicated to delay-trigger mode and about-trigger mode. Figure shows the four different trigger modes.



Trigger Modes

- **Start Trigger Acquisition Mode**

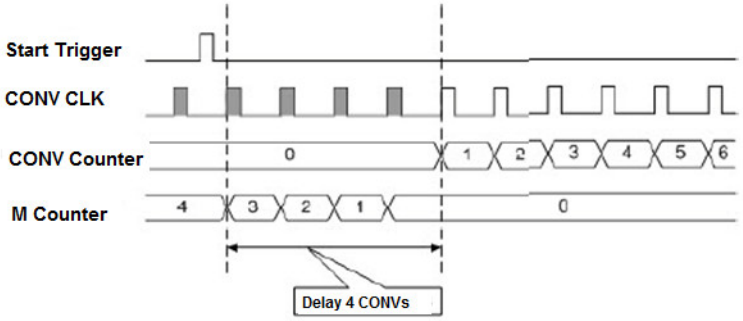
  Start trigger acquisition starts when the PCIE-1813 detects the trigger event and stops when you stop the operation. The CONV CLKs before Trigger will be blocked out. You can set post-trigger acquisition mode by software.



Start Trigger (M = 0)

Delay to Start Trigger Acquisition Mode

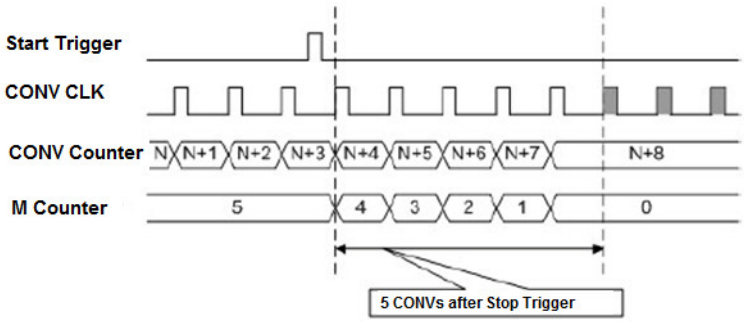
In delay to start trigger mode, data acquisition will be activated after a preset delay number of CONV CLKs has been taken after the trigger event. User can set the delay number of CONV CLKs by a 24-bit counter. Delay to start trigger acquisition starts when the PCIE-1813 detects the trigger event and stops when you stop the operation.



Delay to Start Trigger (M = 4)

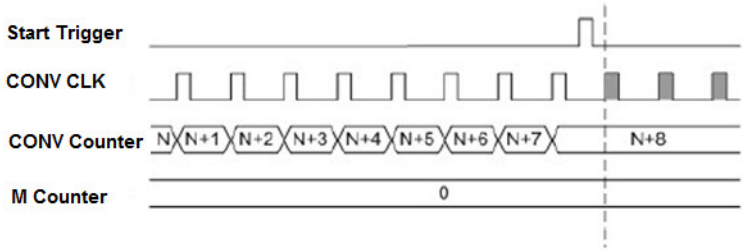
Delay to Stop Trigger Acquisition Mode

If you want to acquire data after a specific trigger event occurs, then you can take advantage of the delay to stop trigger mode. First designate the size of the allocated memory and the amount of samples to be snatched after the trigger event happens. The about trigger acquisition starts when the first CONV CLK signal comes in. Once a trigger event happens, the on-going data acquisition will continue until the designated amount of CONV CLKs have been reached. When the PCIE-1813 detects the selected about-trigger event, the card keeps acquiring the preset number of samples, and keeps them on the buffer.



Stop Trigger Acquisition Mode

Stop trigger mode is a particular application of about-trigger mode. Use pre-trigger acquisition mode when you want to acquire data before a specific trigger event occurs. Stop-trigger acquisition starts when you start the operation and stops when the trigger event happens.



B.1.4 AI CONV Clock Source

The PCIE-1813 can adopt both internal and external clock sources to accomplish pacer acquisition. You can set the clock and trigger sources conveniently by software. The figure can help you understand the routing route of clock and trigger generation.

CONV Clock

- Internal AI CONV clock derived from 32-bit divider
- External AI CONV clock from terminal board

- **Internal AI CONV Clock**
  The internal AI CONV clock applies 100 MHz time base accompanied with 32-bit divider. The maximum frequency is 250 KS/s. According to the sampling theory (Nyquist Theorem), you must specify a frequency that is at least twice as fast as the input's highest frequency component to achieve a valid sampling. For example, to accurately sample a 20 kHz signal, you have to specify a sampling frequency of at least 40 kHz. This consideration can avoid an error condition often know as aliasing, in which high frequency input components appear erroneously as lower frequencies when sampling.

- **External AI CONV Clock**
  The external AI CONV Clock is convenient in uneven sampling internal. AI conversion will start by each arriving rising edge. The sampling frequency is always limited to a maximum of 250 KHz.

B.1.5 AI Trigger Source

The PCIE-1813 supports the following trigger sources for start, delay to start, delay to stop, stop trigger acquisition modes:

- External digital (TTL) trigger
- Analog threshold trigger

With PCIE-1813, user can also define the type of trigger source as rising-edge or falling-edge. These following sections describe these trigger sources in more detail.

- **External Digital (TTL) Trigger**

For analog input operations, an external digital trigger event occurs when the PCIE-1813 detects either a rising or falling edge on the External AI TTL trigger input. The trigger signal is TTL compatible.

- **Analog Threshold Trigger**

For analog input operations, an analog trigger event occurs when the PCIE-1813 detects a transition from above a threshold level to below a threshold level (falling edge), or a transition from below a threshold level to above a threshold level (rising edge). User should connect analog signals from external device or analog output channel on board to external input signal ATRG0/1. On the PCIE-1813, the threshold level is set using a dedicated 16-bit DAC. By software, you can program the threshold level by writing a voltage value to this DAC; this value can range from -10 V to +10 V.

Table B.2: Analog Input Data Format

AI Code		Mapping Voltage	
Hex.	Dec.	Unipolar	Bipolar
0000 h	0 d	0	- FS/2
7FFF h	32767 d	FS/2 - 1 LSB	- 1LSB
8000 h	32768 d	FS/2	0
FFFF h	65535 d	FS - 1 LSB	FS/2 - 1 LSB
1 LSB		FS/65536	FS/65536

Table B.3: Full-Scale Values for Input Voltage Ranges

Gain	Unipolar		Bipolar	
	Range	FS	Range	FS
0.5	N/A	N/A	± 10 V	20
1	0 ~ 10 V	10	± 5 V	10
2	0 ~ 5 V	5	± 2.5 V	5
4	0 ~ 2.5 V	2.5	± 1.25 V	2.5
8	0 ~ 1.25 V	1.25	± 0.625 V	1.25

B.2 PCIE-1813 Analog Output Operation

The PCIE-1813 card provides two 16-bit multi-range analog output (D/ A) channels. This section describes the following features:

- Analog output ranges
- Analog output operation modes
- Synchronous Analog output waveform
- AO clock sources
- AO Trigger sources
- Analog Output Data Format

B.2.1 Analog Output Ranges

The PCIE-1813 provides two 16-bit analog output channels, both of which can be configured internally to be applicable within 0 ~ 5 V, 0 ~ 10 V, ± 5 V, ± 10 V output voltage range. Otherwise, users can use external reference voltage to apply 0 ~ x V or ± x V output range, where the value x is from -10 to +10. Users can configure the output range during driver installation or in software programming.

B.2.2 Analog Output Operation Modes

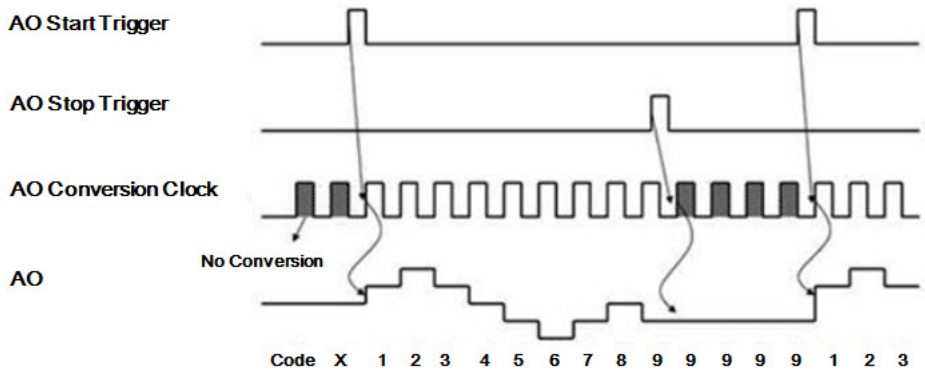
■ Single Value Operation Mode

The single value conversion mode is the simplest way for analog output operation. Users can set the mode of each channel individually. Then users just need to use software to write output data to specific register. The analog output channels will output the corresponding voltage immediately. In the single value operation mode, users need not set any clock source and trigger source, but only output voltage range.

■ Waveform Mode

In waveform mode, all AO channels can change output voltage at the same time. Users can accurately control the update rate (up to 3 MS/s) between conversions of individual analog output channels, and takes full advantage of the PCIE-1813. In this mode you can specify a clock and trigger source and either of the two analog output channels to work in this mode.

Before operating in this mode, users need to set the clock and trigger source first, and then generate the output data stored in the memory buffers of host PC. The host computer then transfers those data to the DACs' buffers on PCIE-1813. When PCIE-1813 detects a trigger, it outputs the values stored in its buffer. When the buffer's storage decreases, the card sends an interrupt request to the host PC which in turn sends samples to the buffer. This output operation will repeat until either all the data is sent from the buffers or until you stop the operation. If the two AO channels are both operating in continuous output mode, the data in buffer will be sent in an interlaced manner, i.e. the "Even-Address" samples in the buffer are sent to AO channel 0, while the "Odd-Address" samples to AO channel 1.



Waveform Mode Output

B.2.3 AO Clock Sources

The PCIE-1813 can adopt both internal and external clock sources for pacing the analog output of each channel:

- Internal AO output clock with 32-bit Divider
- External AO output clock from connector

The internal and external AO output clocks are described in more detail as follows:

- Internal AO Output Clock

The internal AO output clock applies a 100 MHz time base divided by a 32-bit counter. Conversions start on the rising edges of counter output. Through software, user can specify the clock source and clock frequency to pace the analog output operation. The maximum frequency is 3 MS/s.

- External AO Output Clock

The external AO output clock is useful when you want to pace analog output operations at rates not available with the internal AO output clock, or when you want to pace at uneven intervals. Connect an external AO output clock to the pin and then the conversions will start on input signal's rising edge. You can use software to specify the clock source as external. The maximum input clock frequency is 3 MS/s.

B.2.4 AO Trigger Sources

The PCIE-1813 supports External digital (TTL) trigger to activate AO conversions for waveform mode. An external digital trigger event occurs when the PCIE-1813 detects either a rising or falling edge on the External AO TTL trigger input signal from the pin of connector. User can define the type of trigger source as rising-edge or falling-edge by software. The trigger signal is TTL-compatible.

Table B.4: Analog Output Data Format

AO Code		Mapping Voltage	
Hex.	Dec.	Unipolar	Bipolar
0000 h	0 d	0	- FS/2
7FFF h	32767 d	FS/2 - 1 LSB	- 1LSB
8000 h	32768 d	FS/2	0
FFFF h	65535 d	FS - 1 LSB	FS/2 - 1 LSB
1 LSB		FS/65536	FS/65536

Table B.5: Full-Scale Values for Output Voltage Ranges

Reference Source	Unipolar		Bipolar	
	Range	FS	Range	FS
Internal	0 ~ 5 V	5	± 5 V	10
	0 ~ 10 V	10	± 10 V	20
External	0 ~ x V	x	± x V	2x

B.3 Digital Input/Output Operation

The PCIE-1813 supports 32 digital I/O channels. You can use each byte as either an input port or an output port by configuring the corresponding parameter; and all four channels of the byte have the same configuration.

You do not need to specify the clock source or trigger source. To output the data, you just need to write it to the digital output channel directly. In the same way, you can directly read back data from digital input channel. The default configuration after reset sets all the digital I/O channels to logic-low so users don't need to worry about damaging external devices during system start up or reset.

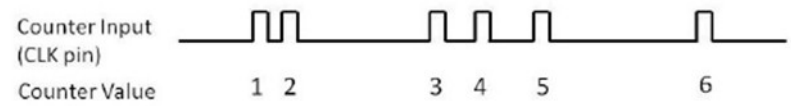
B.4 Counter Input and PWM Input/Output

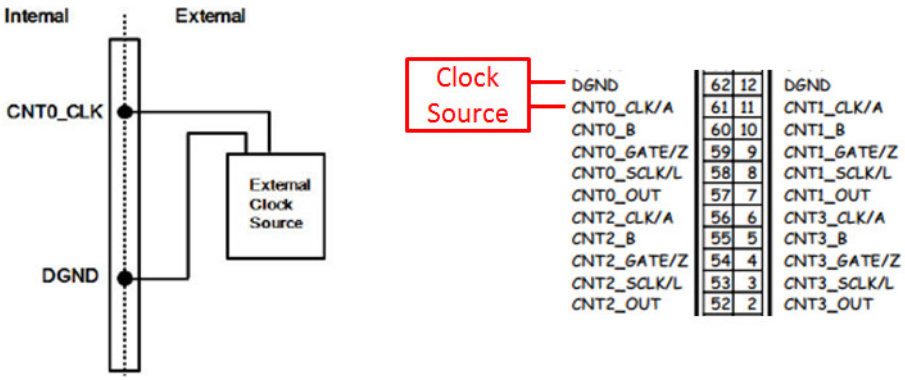
PCIE-1813 offer four 32-bit counters inputs which can perform event counting, frequency measurement, pulse width measurement, and encoder counter with compare output.

Counters on PCIE-1813 have a counter value match interrupt function. When this interrupt function is enabled, an interrupt signal will be generated if the counter value reaches a pre-set counter match value. The counter will continue to count until an overflow occurs, then it will go back to its reset value zero and continue the counting process. A user can set each individual counter channel to count either falling edge (high-to-low) or rising edge (low-to-high) signals.

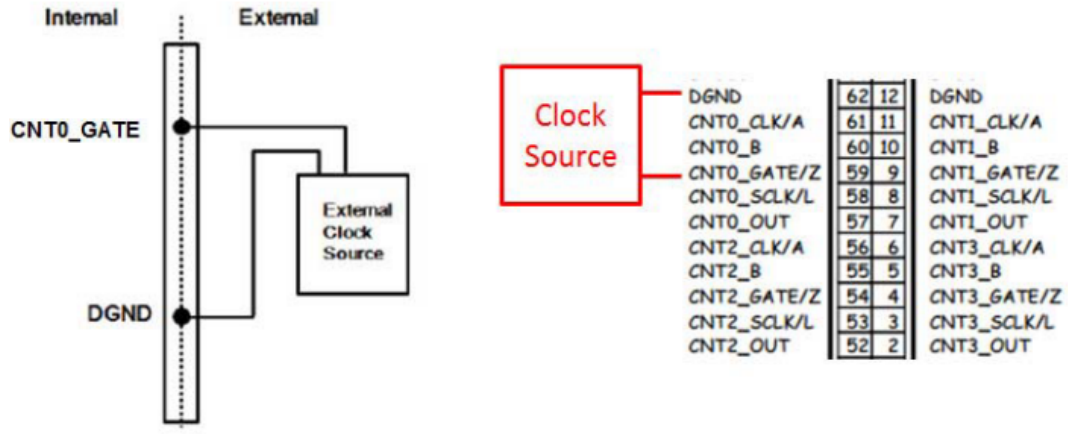
Except measurement functionality, counter input channels can combine with PWM output channels to generate single pulse, pulse train or PWM (pulse-width modulated) output signal. A pulse-width modulated waveform is created when the High and Low periods of a periodic rectangular signal are varied. Using PCIE-1813, user can individually set each PWM channel's High and Low periods for from 2 to (2^{32} -1) units (1 unit = 50 ns), depending on his needs.

1. **Event Counter Connection**
   PCIE-1813 built-in counter can calculate how many pulse are sent into the input channel.

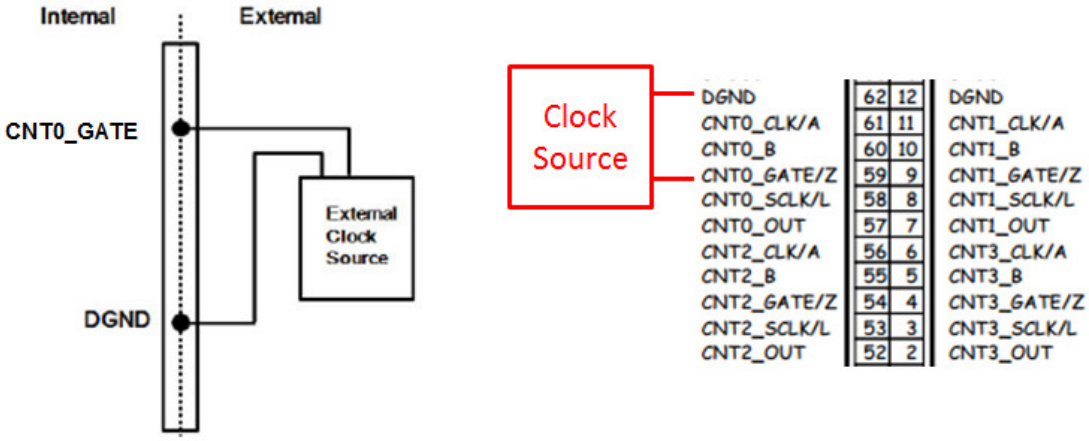




2. **Frequency Measurement Connection**
PCIE-1813 built-in counter can measure the frequency value of the signal connected to counter input. The measurable maximum frequency is 20 KHz with a frequency error smaller than 1%.

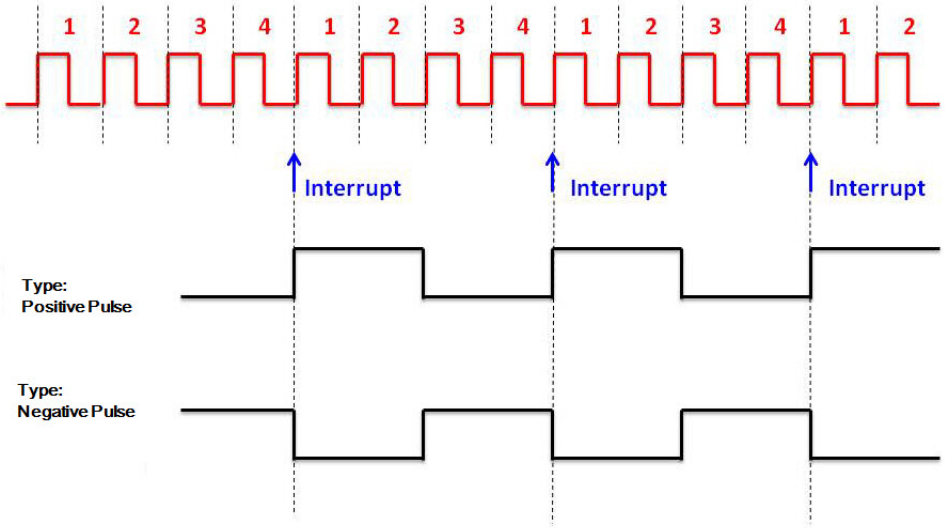


3. **Pulse Width Measurement Connection**
PCIE-1813 built-in counter can measure the pulse width value of the signal connected to counter input. The measurable range is 50 ns to 107 seconds. You can measure both the logic high time and logic low time within the measurable range.



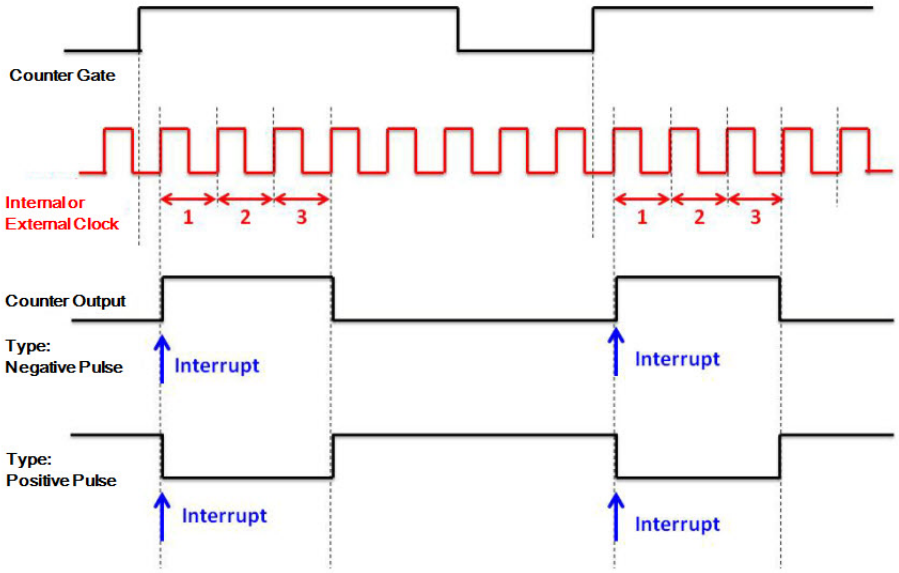
4. **Pulse Output with Timer Interrupt**

PCIE-1813 counter has internal clock that you can produce periodic output signal with interrupt generated at the same time. PCIE-1813 counter will use internal clock as time base, to fulfill the frequency you want to set. See the figure below as example, the desired frequency is 5 MHz. The internal clock is 20 MHz, so PCIE-1813 will periodically generate output signal and interrupt every 4 pulses of the internal clock. (20 MHz / 5 MHz = 4). Available output frequency range is 0.005 Hz ~ 5 MHz.

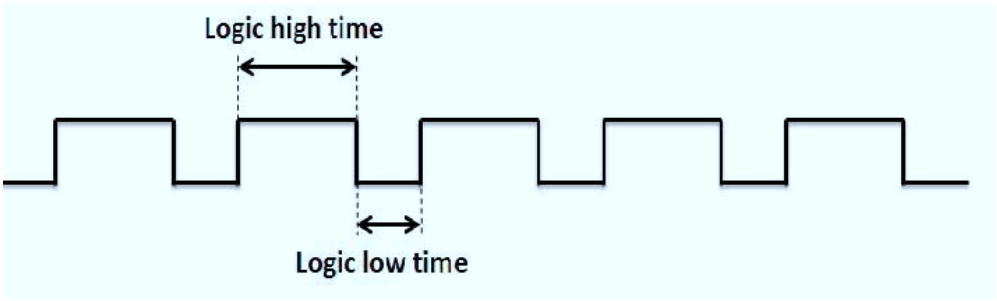


5. **Delay Pulse Generation**

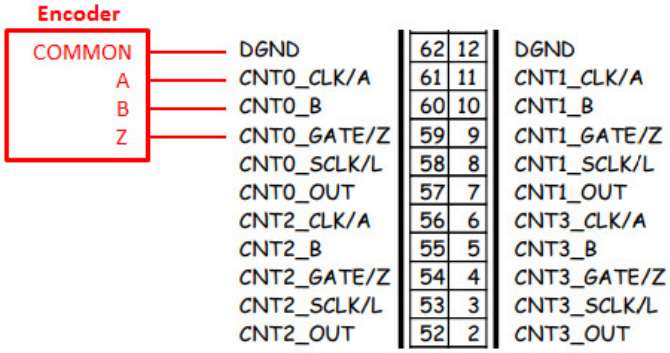
Using PCIE-1813 internal clock, you can change the logic level within a specific period, starting from a trigger signal connecting to counter gate input. For example, if you define the count equals to 3 (as figure below), a counter output will change its status after 3 pulses of internal clock signals pass, after a trigger signal from counter gate becomes high.



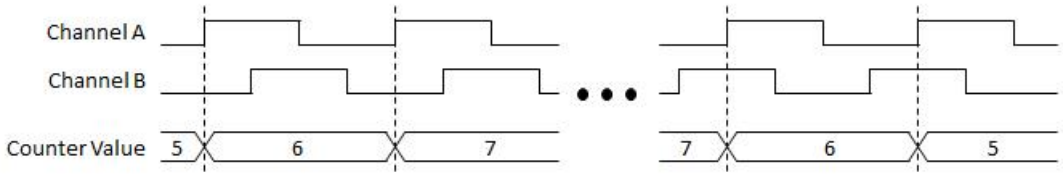
6. **PWM Output:** PCIE-1813 can generate PWM (pulse width modulation) signal which you can configure its logic high time and logic low time as figure below. The available period range for logic high time and logic low time is 100 ns ~ 214 second.



7. **Measurements Using Quadrature Encoders**
The counters can perform measurements of quadrature encoders that use X1, X2, or X4 encoding. A quadrature encoder can have up to three channels: channels A (Source), B (Aux), and Z (Gate).

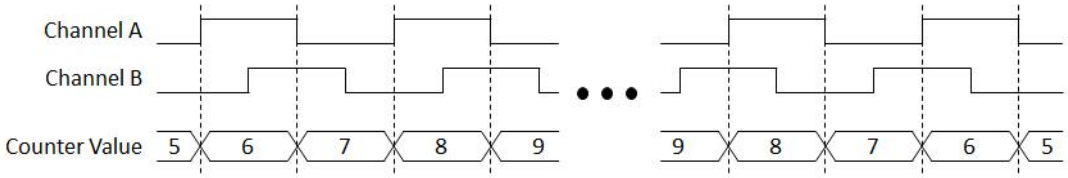


– X1 Encoding: When channel A leads channel B in a quadrature cycle, the counter increments. When channel B leads channel A in a quadrature cycle, the counter decrements. The amount of increments and decrements per cycle depends on the type of encoding (X1, X2, or X4).
Below figure shows a quadrature cycle and the resulting increments and decrements for X1 encoding. When channel A leads channel B, the increment occurs on the rising edge of channel A. When channel B leads channel A, the decrement occurs on the rising edge of channel A.

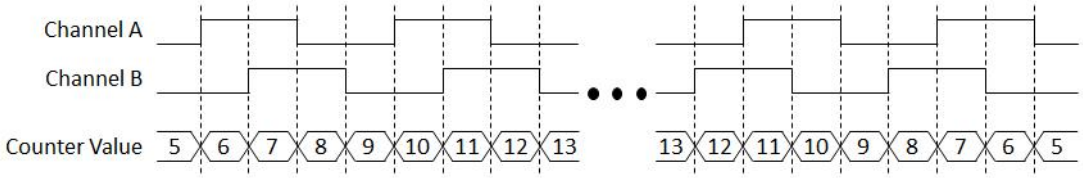


–
–
–
–
–
–

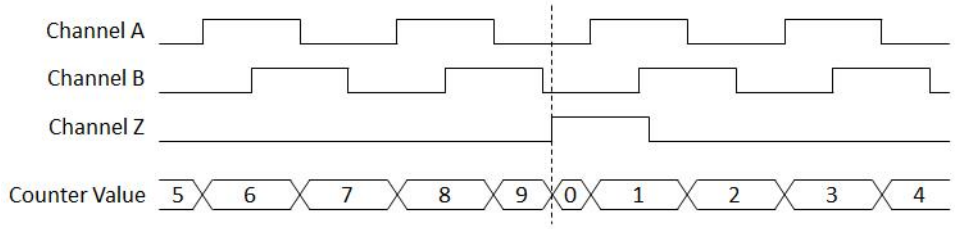
– X2 Encoding: The same behavior holds for X2 encoding except the counter increments or decrements on each edge of channel A, depending on which channel leads the other. Each cycle results in two increments or decrements, as shown in following figure.



– X4 Encoding: Similarly, counter increments or decrements on each edge of channel A and B for X4 encoding. Whether the counter increments or decrements depends on which channel leads the other. Each cycle results in four increments or decrements, as shown in below figure.



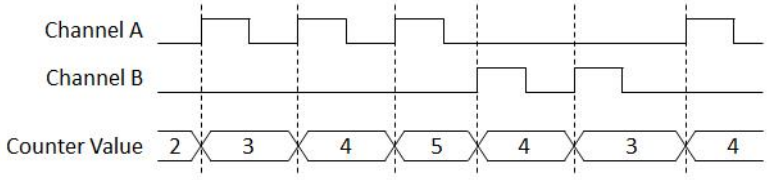
Some quadrature encoders have a third channel, channel Z, which is also referred to as the index channel. According to the configuration, a rising or falling edge of channel Z causes the counter to be reloaded with a specified value. After the reload occurs, the counter continues to count as before. The following figure illustrates channel Z rising edge reload with X2 encoding.



8. **Measurements Using Two Pulse Encoders**

The counter supports two pulse encoders that have two channels: channels A (Source) and B (Aux).

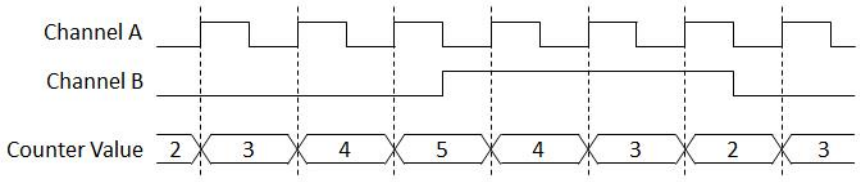
The counter increments on each active edge of channel A. The counter decrements on each active edge of channel B, as shown in below.



9. **Measurements Using Signed Pulse Encoders**

The counter supports signed pulse encoders that have two channels: channels A (Source) and B (Aux).

The counter increments on each active edge of channel A when channel B is low. The counter decrements on each active edge of channel A when channel B is high. This is shown in below.

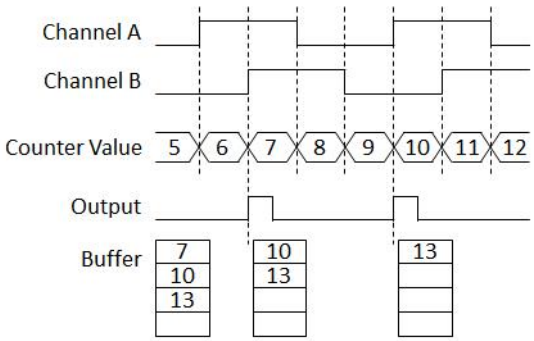


10. **Position Comparison**

This function compares the counter value to a predetermined value. It generates a pulse at Counter Output signal when the counter value becomes equal to the predetermined value. You can define multiple values to be compared and store them in the FIFO. When the counter value becomes equal to the first value in the FIFO, a pulse is generated. In addition, the second value in the FIFO becomes the value to be compared next time.

You can program the width of the generated pulse. The range of the pulse width is from 10 ns to 42.94967295 s in step of 10 ns.

The following figure shows an example of position comparison using quadratureX4 encoding.



ADVANTECH

Enabling an Intelligent Planet

www.advantech.com